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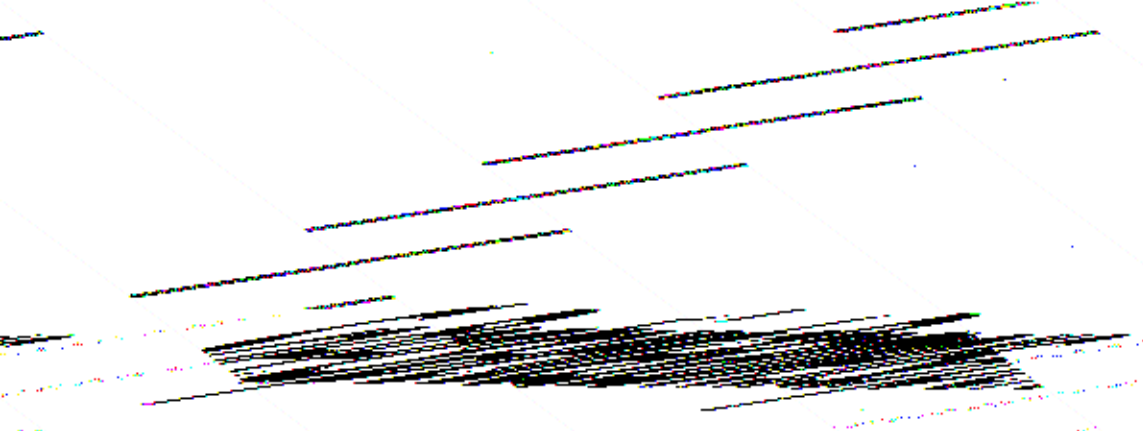
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Visit our technical sessions to learn more:

- TSMC 16nm FinFET SRAM Design Verification
- Impact of FinFET Technology on Physical IP Development, Design Styles, Performance
- FinFET Modeling and Extraction Solutions for TSMC's Advanced 16nm Process
- Design Optimization Kits: Physical IP Solutions for Optimizing CPU/GPU Core Implementations

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EDA Track

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Managing Wire Resistance, Cell Pin Access and FinFET Parasitics at TSMC 16nm Using Cadence Place & Route and RC Extraction Technologies

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ABSTRACT

At 20nm and 16nm design rule complexity makes it very difficult for routers to connect efficiently to pins on standard cells. As a result, careful control of pin densities during cell placement and global pin access planning during detail routing can have a big impact on acheivable design area. Also, with wire resistances continuing to rise exponentially, effective use of low resistance high metal layers to buffer timing critical nets is vital to achieve good timing closure.

Parasitic extraction for FinFET is significantly different from regular planar CMOS devices. 3D FinFET models introduce challenges in capacitance modeling, since it involves gate, fins and external contacts. FinFET gate to source/drain capacitances are more complex than regular FETs. Furthermore, there are resistance modeling challenges due to non-uniform current distributions, requiring advanced modeling techniques for accurate resistance.

This paper shows how the Cadence Encounter P&R and QRC Extraction solution comprehensively manages pin access through the flow, automatically leverages high metal layers timing optimization, and supports FinFET devices, to improve frequency, power and area at TSMC 20nm and 16nm process nodes.



Resistance, Pin Access & FinFET Parasitics

Achieving best results using Cadence place & route and RC extraction solutions on TSMC 16nm

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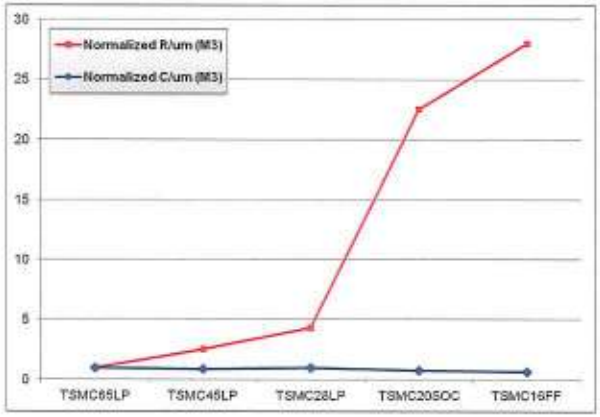
Agenda

- Resistance trend and its impact on timing closure
- Cadence route-driven optimization technology
- Design rule complexity and its impact on routing closure
- Cadence pin access-driven design flow technology
- FinFet parasitic extraction challenges
- Cadence QRC extraction solution

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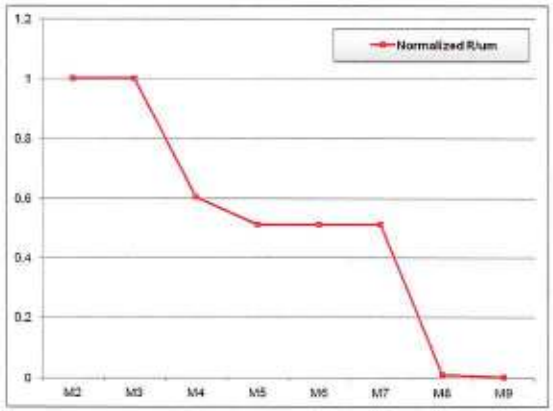
Wire resistances rising exponentially



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Variable thickness metal stacks essential



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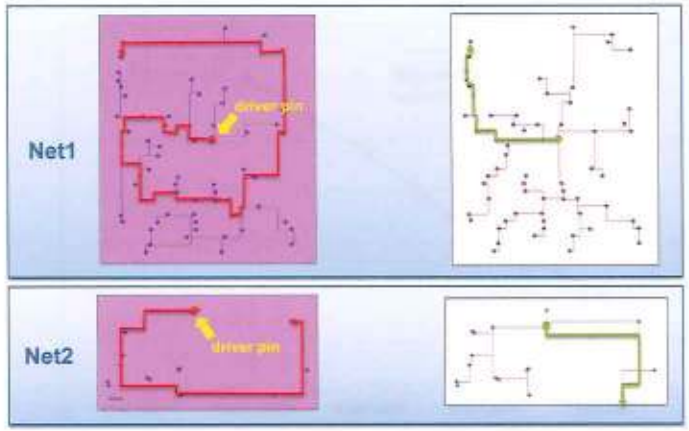
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Best buffering depends on layer and NDR

Layers	NDR	Best Drive Strength	Normalized repeater spacing	Normalized driving speed
M2,M3	1xW 1xS	X8	1.00	1.00
M4,M5	1xW 1xS	X12	0.82	1.57
M6,M7	1xW 1xS	X12	0.86	1.59
M2,M3	2xW 2xS	X16	1.49	2.53
M4,M5	2xW 2xS	X12	1.55	2.68
M6,M7	2xW 2xS	X16	1.23	2.76

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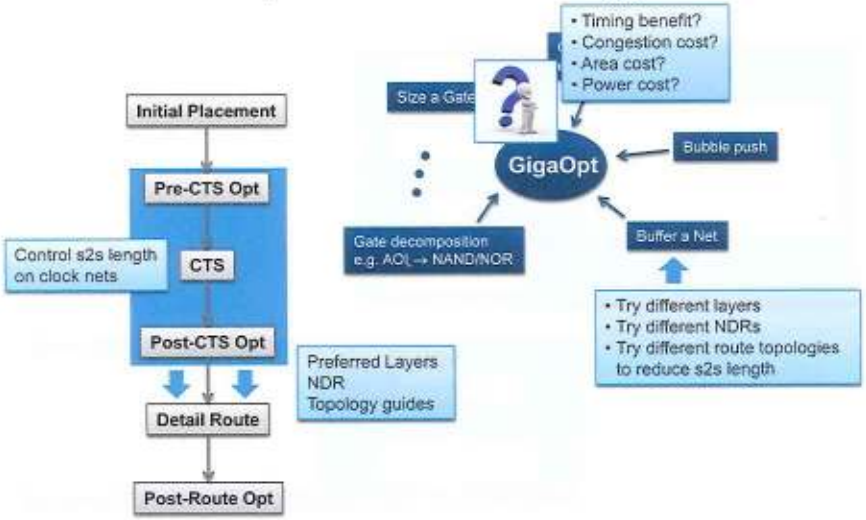
Resistance depends on wire topology



Total net length similar but worst source2sink length very different

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Route-driven optimization technology



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Example results

Quad-core ARM Cortex-CA15 at TSMC 16FF

	Post-route
WNS (ns)	-0.194
TNS (ns)	-99
FEP	3,050

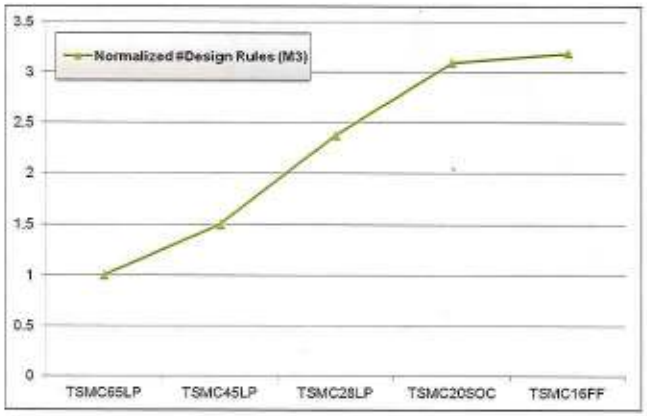
With route-driven optimization

	Post-route
WNS (ns)	-0.273
TNS (ns)	-195
FEP	5,793

No route-driven optimization

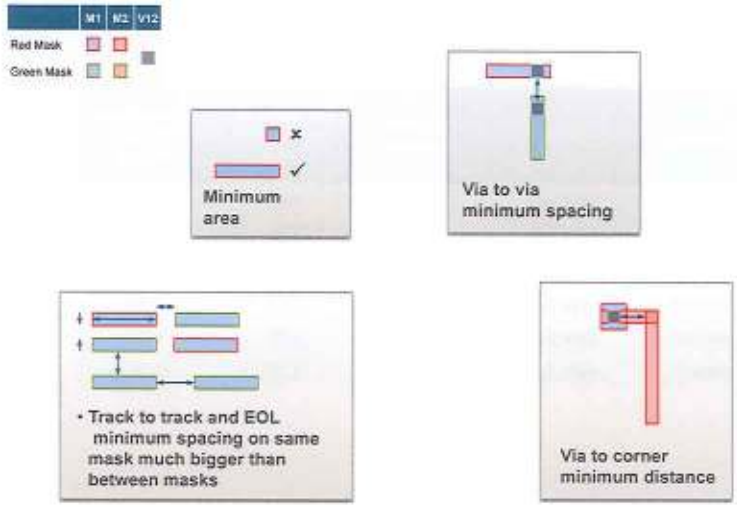
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Design rule complexity rising rapidly



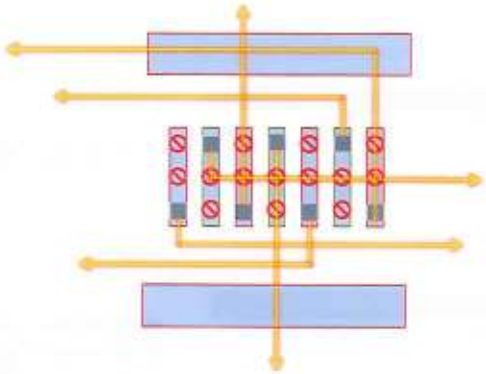
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Pin access is a new critical design closure metric



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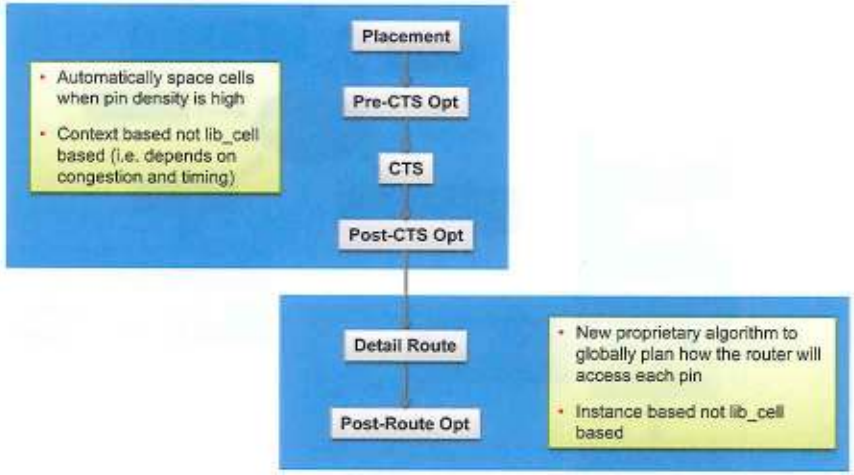
Pin access is a new critical design closure metric



May be impossible to route even if congestion is low

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Cadence pin access driven design flow



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Example results

Quad-core ARM Cortex-CA15 onTSMC 16FF

	Post-route
WNS (ns)	-0.045
TNS (ns)	-32
FEP	2,500
Utilization	61%
DRC	85

With auto pin spread

	Post-route
WNS (ns)	-0.111
TNS (ns)	-262
FEP	11,727
Utilization	61%
DRC	95,081

No auto pin spread

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RC Extraction

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Key challenges

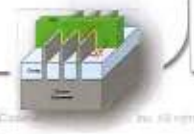
1. **Introduction of new and additional parameters e.g Cgs, Res, that requires complex modeling for better accuracy**
2. **Explosion in parasitics results in bigger netlist impacting post-layout simulation performance and requires faster TAT for digital designs**
3. **Designers need can no longer afford to wait and see impact of parasitics post-layout simulation— early assessment during schematic simulation is required for better design convergence**
4. **Deep integration of signoff extraction in P&R for better post-route optimization, better TAT with incremental extraction and better convergence to signoff with metal fill estimation**

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Parasitic challenges—capacitance, resistance

- Dominated by fringe 3D capacitances from gate, fins etc.
- Gate thickness introduces new capacitances components to fins (s/d)
- External capacitances to M0/V0 (MEOL) contacts

Ring Oscillator	Number of C (Cc)
28nm	Y
16/14nm	45Y



- Explosions of R and hence better handling techniques required to expedite post layout simulation
- Model three different resistance types
 - Contact Resistance
 - Spreading Resistance
 - Extension Resistance

Ring Oscillator	Number of Rs
28nm	X
16/14nm	155X



- **Biggest impact is below Metal 1**
- FEOL features
 - Multi-finger fins per device with varied pitches and widths
 - Complex poly structures
 - Other features similar to 20/28nm
 - Raised source drain
 - 2-step M0
 - Fracture via, etc.
- Current FF processes have similar BEOL DPT modeling requirements
 - Litho bias
 - DPT corner variations
 - DPT mask shift variations



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Parasitic Challenges—lack of convergence between pre-post layout simulation

- Device parasitic RCs impact circuit timing
 - Impacts become stronger as devices become smaller
- STD cells study
 - Shows up to 20%—67% increase in delay with pre-sim and post-simulation

20nm Std. Cells	Post-sim(ns)	Pre-sim(ns)	Delay Increase
Design 1	0.1603	0.1235	29.8%
Design 2	0.1085	0.0904	20.0%
Design 3	0.2465	0.175	40.9%
Design 4	0.1538	0.121	27.1%
Design 5	0.2154	0.168	28.2%
Design 6	0.2357	0.189	24.7%

16nm Std. Cell	Post-sim(ns)	Pre-sim(ns)	Delay Increase
Design 1	$2.35e^{-11}$	$1.48e^{-11}$	55.4%
Design 2	$3.78e^{-11}$	$2.32e^{-11}$	62.9%
Design 3	$5.67e^{-11}$	$3.44e^{-11}$	64.8%
Design 4	$5.73e^{-11}$	$3.44e^{-11}$	66.6%

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Tighter MOS and ring ossicelator accuracy vs. reference data

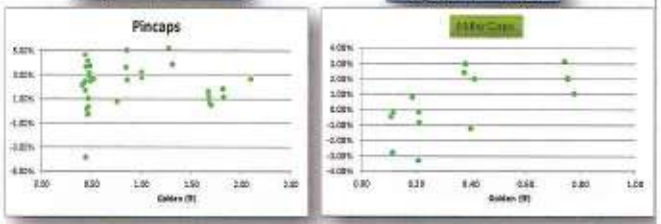
- MOS accuracy

Mean	-0.4%
Sigma	1.4%

- Pin caps and Miller caps accuracy

Mean	2.1%
Sigma	1.7%

Mean	0.7%
Sigma	1.8%



- Accuracy vs. golden

	Ref. Data	PVS+QRC	
freq (=10/period) (GHz)	3.694	3.608	-2.328%
tp (ns)	0.1835	0.1789	-2.507%
tn (ns)	0.1859	0.1819	-2.152%
duty = (100*tp)/(tp+tn)	49.674	49.566	-0.217%

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Faster characterization of std. cells, SRAMs, and IP using QRC extraction

- Example using VCO to show QRC's ability to do characterization faster with the same accuracy as field solver
- Net list size comparison
 - 2X smaller net list than competition
- Best QRC net lists simulation run times
 - 2.5x faster than competitors' VCO simulations

VCO-Ring	Ref. Data (Field Solver)	Competition	PVS + QRC
RC Extraction Time (Real Time)	22days,7 hrs,58min	1min	3min
RC Netlist Size (Mb)	4.8	6.4	3.2
Simulation Run Time (hrs)	3.08	4.34	1.71

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EDI-QRC integration
Best turnaround time & convergence

EDI Digital Implementation Timing/SI Optimization

Turbo QRC (TQRC)
- Near signoff quality
- Upt o 2-3x faster than signoff
- Multi-corner extraction

Same QRC Engine

Integrated QRC (IQRC)
- Used for ECOs/incremental extraction
- Faster than signoff—extract only changed nets
- Used for accurate CLK/NDR nets for 28nm designs and below
- Multi-corner extraction

Signoff Extraction

Signoff QRC
- Full blown, foundry qualified including QRC field solver (QRCFS)
- Multi-corner extraction

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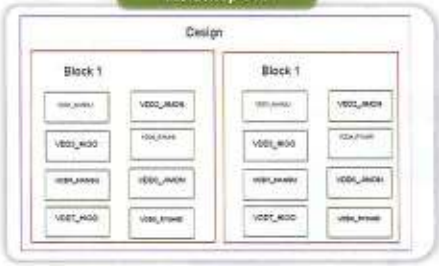
Incremental Extraction in Encounter improves Signoff Flow TAT

1. Eliminates full flat extraction for functional ECOs at block level and full chip
2. Better signoff TAT during chip finishing level
3. As accurate as standalone signoff full chip extraction including metal fill

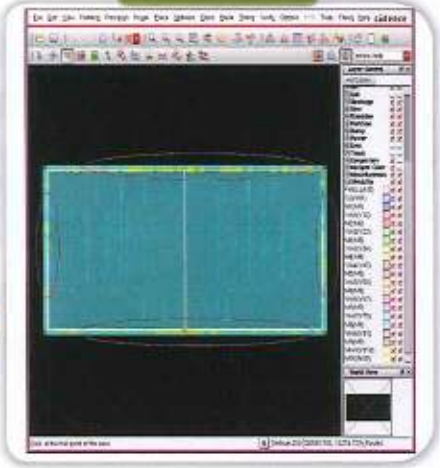
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Customer evaluation results

200 random selected ECO nets are changed inside top cell



28nm—36M Nets



	Full Run	ECO Run	Speed Up	# of CPUs
TAT (mins)	1224.16	332.85	3.67X	16

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QRC extraction—complete FinFET extraction solution

- Collaborated with TSMC to deliver parasitic models
- Key differentiators
 1. Tight accuracy vs. reference
 - Built upon robust 3D modeling framework
 - Best cap. and timing accuracy vs. TSMC Golden
 2. Faster post layout simulation turnaround time (TAT) and digital designs TAT
 - Best net list size and simulation time for a VCO design
 - 2X smaller net list
 - 2.5X faster simulation runtime
 - 4X better performance with MF on 16CPUs
 3. Tight integration in Encounter and Virtuoso for faster design convergence



QRC extraction & QRC field solver (QRCFS)

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Design Reliability with Calibre® YE-SmartFill and Calibre® PERC™

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ABSTRACT

The complexity of advanced technologies drives new requirements for poly/OD and metal fill to solve critical manufacturing effects, and more importantly design yields. New methodologies were developed for 28nm designs using Calibre SmartFill to meet the new strict DFM requirements while reducing run time, file size and iterations.

Besides manufacturing process, electrical rule checks can also significantly impact design yields & reliability. Identifying incorrectly configured devices, multi-power domain transition guides, and floating (leaky) gates is critically important right from the circuit stage, well before physical layouts. Such early design consistency checks written with rules in Calibre® PERC™ help us catch design mistakes early on, and validate some of our high reliability design metrics.

Both Calibre Smart-Fill and Calibre® PERC™ were significantly and successfully deployed on Broadcom's largest 28nm tapeout recently, which the Broadcom representative will describe in the presentation.



Design Reliability with Calibre® YE-SmartFill and Calibre® PERC™

Muni Mohan
I.C. Design Manager
Processor & Wireless Infrastructure
Broadcom Corporation

BROADCOM.

Jeff Wilson
YieldEnhancer Product Marketing Manager
Mentor Graphics

Mentor Graphics

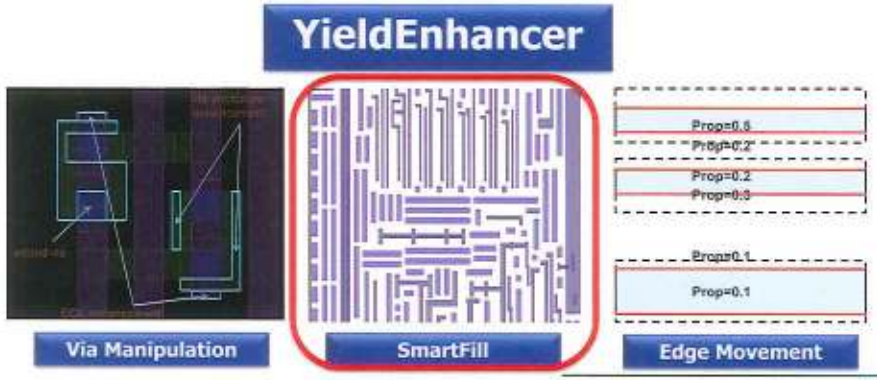
Agenda

- Current status at TSMC
 - Calibre® YieldEnhancer™ SmartFill functionality
 - Calibre PERC functionality
- Broadcom's experience
 - Chip Description
 - Calibre PERC usage and driving factors
 - Calibre YieldEnhancer SmartFill usage and driving factors
- Summary

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Calibre YieldEnhancer
Improves Design Robustness with Flexibility

- YieldEnhancer provides
 - Multiple types of modifications
 - Fits in multiple design environments



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SmartFill Decks at TSMC

- 65nm/55nm: Both FEOL and BEOL decks
- 45nm/40nm: Both FEOL and BEOL decks
- 28nm: FEOL deck includes both digital & TSMC 1st analog fill deck
- 20nm: Both FEOL and BEOL including double patterning (DP)
- 16nm: Both FEOL and BEOL including DP and FinFET


Mentor Graphics Design, and Verification Tools Certified for TSMC 16nm FinFET

WILSONVILLE, Ore., May 28, 2013— Mentor Graphics Corp. (NASDAQ:MENT) to

The Calibre nmPlatform product for 16nm FinFET supports adva
hotspot pre-filtering. In addition, the Calibre SmartFill facility was
transistors, including support for density constraints and multila
double patterning support for back end layers and user-defined
design.

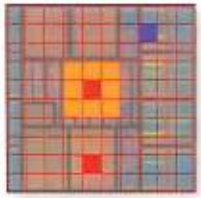
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Mentor Graphics' Calibre SmartFill Addresses TSMC 20nm Fill Requirements

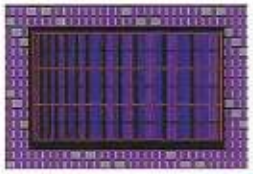
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SmartFill's Analysis Engine
Provides a Correct by Construction Solution

- Delivers the correct results by combining analysis with the filling operation
 - — SmartFill supports all density constraints
 - – Local (Absolute Constraints)
 - – Short Range (Gradient Constraints)
 - – Long Range (Magnitude Constraints)
 - – To Max option

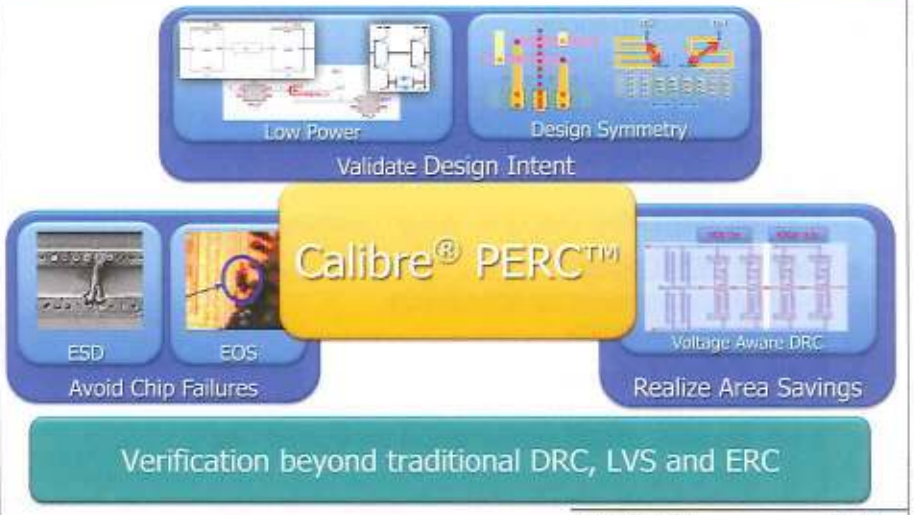


- Analysis engine creates a correct by construction analog fill solution
 - — Fill uniformity improves transistor performance uniformity
 - – Create fill to match the design
 - — Analysis-driven Fill
 - – Multiple layers to consider for analysis
 - – Multiple layer fill structures need to be inserted
 - – Balancing is by layer



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Calibre PERC
A New Approach To Circuit Verification



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Calibre PERC
TSMC ESD/LUP Decks



- ESD/Latch-Up rules
 - — Rules in the Design Rule Manual
 - — 65% can be checked but tedious, 35% are un-checkable
- MGC/Calibre collaboration delivers robust verification
 - — No competitive offering for both netlist and layout solutions
- 28nm/20nm ESD/LUP decks available for download

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Agenda

- Current status at TSMC
 - — Calibre YieldEnhancer's SmartFill functionality
 - — Calibre PERC functionality
- Broadcom's experience
 - — Chip description
 - — Calibre PERC usage and driving factors
 - — Calibre YieldEnhancer SmartFill usage and driving factors
- Summary

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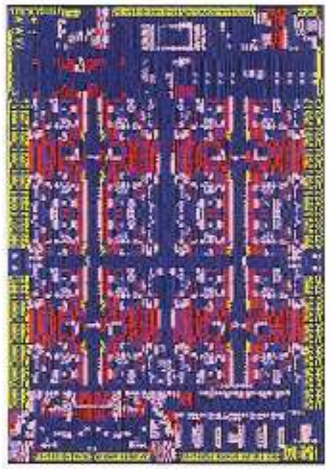
Salient Features
Our largest CPU chip required new tools & approaches

- Calibre YieldEnhancer
 - — SmartFill used on both FEOL and BEOL including ICOVL and TCD cell insertion
 - — SmartFill based hierarchical trench fill for inter-block channels
 - — SmartFill based via-punch for power grid fortification
- Calibre PERC
 - — Customized PERC checks for design reliability
- Calibre DESIGNrev™
 - — Window-Clip based top-level debug
 - — Chip level assembly
- Design Flow Changes
 - — Compressed Oasis file-format used extensively
 - — Deployment of DRC waiver flow in the sign-off loop

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Features of our Largest CPU Chip

- Largest multi-processor chip done by our division
 - — Using TSMC28-HP
- Several billion transistors
 - — Verified by Calibre
 - — Using MT-Flex on a dedicated 208 CPU grid controlled by LSF



** Intentional modification of aspect ratio*

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Calibre PERC Usage
Compelling factors

- Calibre PERC checked specific rules previously un-checkable with conventional DRCs
- Check examples
 - — High-Voltage Differential Checks – with limited false-flags
 - – Much cleaner, better & faster than flag based DRCs
 - — MOS devices with "Reliability Failure-prone" supply hookups
 - — Floating Gate Checks – based on actual connectivity
 - – Cleaner and faster than the false-error prone PO.R.19 DRC check
 - — Schematic only reliability checks
 - — Bus-Bit Squiggle checks
 - — Crow-bar shunt connected MOS checks
 - – No false flags unlike the ERC_WELL_TO_PG_CHECK

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Calibre PERC Usage
Performance

- All checks were developed in-house
 - — Over one dozen checks, full-chip
- Great runtime and memory
 - — Runtime: ~32 minutes
 - — Memory: 52 Gig

```
--- CALIBRE::PERC EXECUTIVE MODULE COMPLETED.
    CPU TIME = 1874  REAL TIME = 1921
    LVHEAP = 44512/51581/51584  MALLOC = 52780/52780/52780
    ELAPSED TIME = 1921

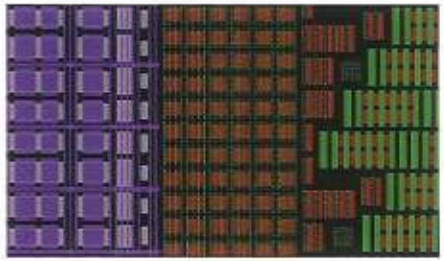
--- CALIBRE::PERC CHECK(s) PASSED

--- TOTAL CPU TIME = 1874  REAL TIME = 1921
    LVHEAP = 44512/51581/51584  MALLOC = 52780/52780/52780
    ELAPSED TIME = 1921
```


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Calibre YieldEnhancer FEOL Deck

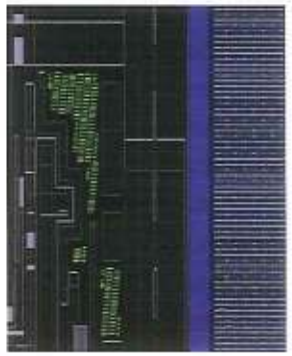
- Utilized TSMC online FEOL SmartFill deck
 - — Correct by construction fill
 - – Analyzes the design as it fills
 - — Utilizes cell-based fill functionality
 - – Multi-layer fill shapes
 - – Reduces run time
 - – Reduces file size
 - — Supports both GDS & OASIS
 - — Supports very large designs
 - — TCD/ICOVL cell insertions



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Calibre YieldEnhancer BEOL Deck

- Broadcom looked to SmartFill for their TSMC 28nm BEOL solution for the following reasons
 - — Previous fill approach had gradient violation issues
 - — Minimize the timing impact of fill
 - — Reduce run time and file size
- SmartFill delivered
 - — Gradient analysis is part of SmartFill and the design was 100% density clean
 - — SmartFill timing impact is less than previous designs using OPC wrap fill
 - — Largest block completed in ~1 hour
 - — 20x file size reduction
 - — Macros made deck development easy to build and maintain
 - — Fit our design methodology



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Agenda

- Current status at TSMC
 - — Calibre YieldEnhancer's SmartFill functionality
 - — Calibre PERC functionality
- Broadcom's experience
 - — Chip Description
 - — Calibre PERC usage and driving factors
 - — Calibre YieldEnhancer SmartFill usage and driving factors
- Summary

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Next Generation Chip and Technology
Continuing Our 3-Way Relationship

- Continue our successful 3-way relationship
 - — Problem is not getting easier
 - — Larger designs at new technologies include
 - – Double patterning and FinFET requirements
- Broadcom looks forward to utilizing TSMC supported decks in future technologies
 - — Both FEOL and BEOL SmartFill decks are available at 20 and 16nm
 - — PERC decks are available for a number of checks at 28 and 20nm
- Work needs to go beyond decks into design methodology
 - — Hierarchical approach to fill is recommend because it impacts Fill run time and post Fill DRC run time
 - — ECO Fill flow announced in 16nm Reference Flow
 - — Sign-off PERC checks – for design reliability and leakage

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TSMC 16nm FinFET SRAM Design Verification

Synopsys

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

Continue scaling of embedded SRAM into the 16nm technology node and beyond is critical for applications ranging from high-performance computing to low-power mobile devices. For 16nm technology node, the emergence and use of FinFET 3D transistor bring many new opportunities to the SRAM design, but it also accompanies with new challenges to the SRAM design verification. Due to the FinFET 3D structure, the model complexity and device parasitics have increased significantly, along with device width quantization, layout rules and extraction complexity increased. The insatiable low power and stringent read/write stability requirements in advanced FinFET SRAM require innovative power management circuits and read/write assist schemes to increase circuit operating efficiency and stability. In addition, with FinFET's higher driving strength, IR/EM analysis becomes increasingly important to ensure final SRAM design reliability.

To address these challenges and enable efficient FinFET SRAM design, Synopsys and TSMC came forward by closely collaborating on enhancing SPICE and FastSPICE tools. Through FinFET BSIM-CMG model validation, IR/EM rules certification, SRAM instance pre-layout and post-layout timing and power simulation calibration and IR/EM simulation verification, the teams have established a working productive flow for 16nm-FinFET SRAM design verification.

This paper will first review how TSMC and Synopsys jointly implement and optimize TSMC FinFET device model through HSPICE simulator. This will be followed by discussion on pre-layout and post-layout timing and power simulation accuracy validation process and simulation technology enhancements. PODE device back annotation support for post-layout simulation will also be covered. Finally, new DC/AC EM rules calibration process, direct IRCX support and SRAM instance IR/EM analysis will be presented.



TSMC 16nm-FinFET SRAM Design Verification

Antony Fan, Mark Han, Amelia Shen, Weidong Liu, Vladimir Aptekar, Yen-Huei Chen*, Wei-Min Chan*, Hung-Jen Liao* Jonathan Chang* and Frank Lee

(Synopsys, Inc.; *: TSMC)

October 2013

Agenda

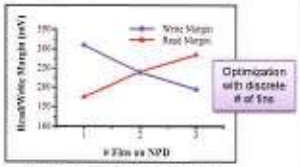
- 16nm-FinFET SRAM Design Challenges
- Establish 16nm-FinFET SRAM Design Verification Flow
 - SPICE Model Optimization
 - Parasitic Back Annotation Adjustment
 - Circuit Simulation Validation
 - IR/EM Simulation Verification
- Summary

FinFET Design Impacts

- Current driving strengths are quantized
 - No continuous sizing to optimize circuits
 - Read/write assist circuitry is a must
- BSIM-CMG model evaluation is more expensive than BSIM4
 - More impact on equation model
 - Less impact on table model.
- Much more complex parasitic R's and C's due to 3D transistor architecture and M0/Trench contacts
 - Longer simulation time
- P-MOSFET and N-MOSFET have about equal driving strengths
 - Symmetric rise/fall times
- Less body effect



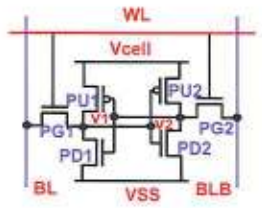
Source: TSMC IEDM 2010

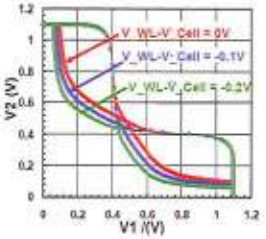


Source: Prof. Tsu-Jae King Liu, UC Berkeley

16nm SRAM Circuits Design and Verification Challenges

- **Increasing power network circuitry complexity**
 - Power gating to reduce leakage currents
 - Read/write assist circuits to change Vcell/WL during read/write cycle to improve Static Noise Margin (SNM)
- **Increasing parasitic Rs and Cs**
 - Local interconnects (M0) and trench contacts increase parasitic R's and C's and the coupling cap between source/drain and gate terminals of the transistors
 - 3D FinFETs
- **Increasing IR drop impact**
 - SNM is sensitive to IR drop due to the use of multiple level Vdd
- **Increasing number of corners for verification**
 - Power management circuits uses multiple operating voltages
- **Increasing reliability problems (EM, HCI, NBTI, PBTI)**

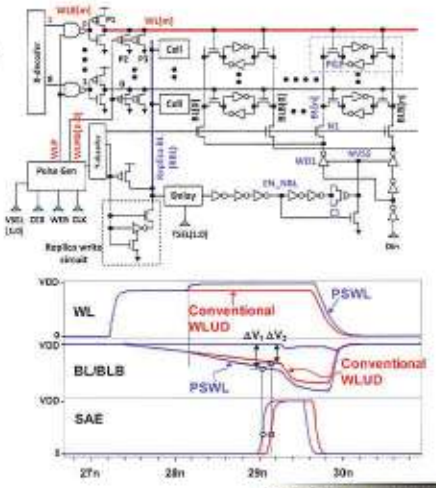




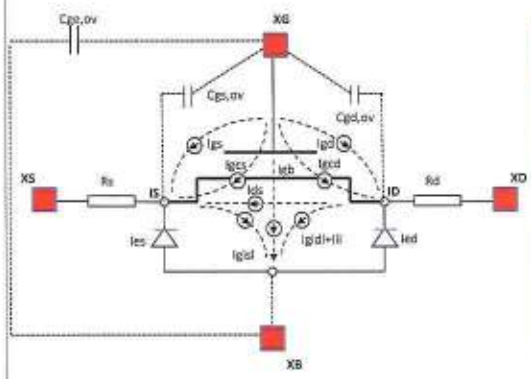
Improved Read Margin

16nm-FinFET SRAM Circuit Simulation Needs

- Device Model Optimization
 - BSIM-CMG for TSMC 16nm-FinFET
 - Model optimization for quality and performance
- 16nm-FinFET Design Parasitic Back Annotation Adjustment
 - Increase number of RC and RCC
 - PODE device back annotation
- Circuit Simulation Validation
 - Verify 16nm-FinFET Device Model simulation accuracy
 - Verify 16nm-FinFET TSMC SRAM instances timing, and power simulation accuracy
- IR/EM Simulation Verification



Synopsys BSIM-CMG for TSMC 16nm FF V0.5



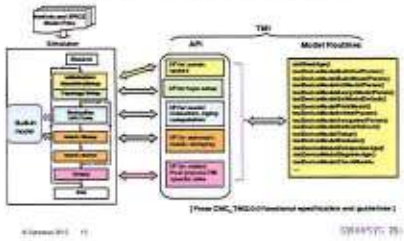
Parasitic R & C		Pre-layout (by BSIM-CMG)	Post-layout (in SPF)
Source & drain resistance	Rd	Y	Y
	Rs	Y	Y
Overlap caps	Cgs,ov	Y	Y
	Cgd,ov	Y	Y
	Cge,ov	Y	Y

- New model formulation based on surface-potential
- Similar model topology as planar BSIM4

In-depth Collaboration with TSMC on 16nnFF SPICE Model – TMI2/ETMI2 API



TMI Architecture and Implementation

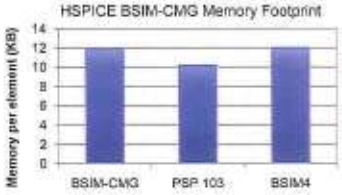


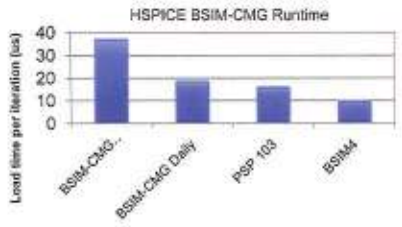
- Jointly developed TMI and ETMI2 modeling to support device LDE, variability, DFM, MOS aging, RDR, SOA, and RF modeling
- Joint developed ETMI2 qualification and release process mechanism

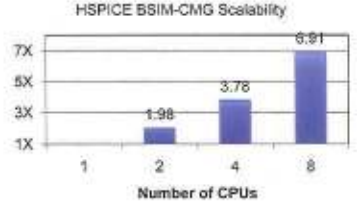
* ETMI2 is TSMC SPICE library release format for N16FF

HSPICE BSIM-CMG 106.1

- 2X performance improvement over 2012.06-SP2
 - 2X slower than BSIM4 because of more complex formulations
- Near linear scalability
- Similar memory footprint as BSIM4







16nmFF Model QA in HSPICE, FineSim and CustomSim

Test suite includes test cases from TSMC and developed by Synopsys

- Unit test
 - P/V/T sweeping
 - Instance and model parameters sweeping
 - Parameter range and numerical FPE checking
 - All model topologies
 - Version control scheme
 - MT thread safety
- OS Platforms
- Analysis type: OP/DC/AC/Tran/Noise/PZ/SN/PN/MC
- Simulator specifics
- Performance, memory



16nm-FinFET Design Parasitic

- 10X increase in the number of RC and RCC in the extraction files
 - Detailed extraction of interconnect layers
 - Detailed extraction of 3D FINFET parasitic R's and C's critical for accurate verification
- PODE device back annotation
 - Additional parasitic device extraction for PODE devices included in the back-annotation flow
- Validate Simulator Accuracy and Performance
 - Advanced handling for parasitic RC's to maintain simulator performance and accuracy tradeoffs with 10X the RC's
 - PODE Device handling for performance and accuracy

16nm-FinFET TSMC SRAM Instances

- Test cases includes pre-layout and post-layout critical path with different size of SRAM instances range from 256x4 to 512x86.
- MOS count ranges from 4.7K to 944K , parasitic RCC count ranges from 38K to 12M.
- Simulation accuracy requirements
 - Timing Measurements: 2% or 2ps vs. HSPICE golden
 - Voltage Measurements: 2% or 2mv vs. HSPICE golden
 - Current Measurements: 5% or 5nA vs. HSPICE golden
- Verified16nm-FinFET TSMC SRAM instances timing, and power simulation accuracy for HSPICE, FineSim and CustomSim in May

IR/EM Simulation Verification

- Covers two areas:
 - EM rule coverage
 - EM/IR accuracy validation
- DRM v.0.5 used as a guide
- EM rules provided as iRCX file: ~5200 line of code
- Reliability Analysis(RA) has a capability to accept EM rules in iRCX file:
 - Ensures correctness of the rules
 - No manual coding of the rules is necessary
 - Eliminates tedious task

EM Rules Coverage

- New 16nm EM rules
 - Electron current direction
 - Power grid rule
 - Middle end of line (vertical and horizontal currents)
 - High-R (functional) resistors
 - Pulse duration and period dependent peak rule
- Simple current density calculation is not enough – also consider local layout context and current values
- 22 test patterns simulated to calculate current limits for ~400 checkpoints
- Accuracy of the I_{avg}, I_{RMS} and I_{peak} current limits validated to be within the TSMC requirements

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EM/IR Accuracy Validation

- TSMC reference test case
 - Inverter chain based clock tree with various wire length and high fanout count
 - Power nets and signal nets extracted RCC (resistors, ground and coupling capacitors)
- Resistor currents and node IR drop at ~2000 checkpoints used as a reference
- Test case netlist simulated in HSPICE to produce reference values
- RA flow executed to generate RA report (IR and EM values)
- Results compared for accuracy validation

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Summary

- 16nm-FinFET provides new opportunity and challenges for SRAM design verification
- 16nm-FinFET SRAM Circuit Simulation Needs
 - Device Model Optimization
 - Design Parasitic Back Annotation
 - Circuit Simulation Validation
 - IR/EM Simulation Verification
- TSMC and Synopsys have established a working productive flow for 16nm-FinFET SRAM design verification.

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Addressing Custom Design Challenges for IP Design at 16nm FinFET Technology

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ABSTRACT

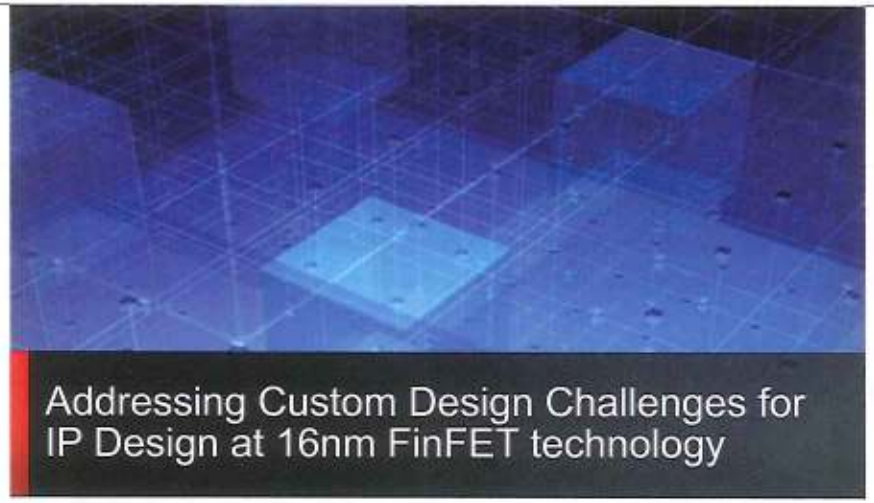
16nm FinFET technology offers great advantages in power and area reduction for digital designs, but escalate challenges in scaling custom circuits due to increased impact of device parasitics and Layout Dependent Effects (LDE), discrete device dimensions and more complex design, electromigration and reliability rules. To address these challenges custom designers need highly integrated flow with new advanced analysis, layout and signoff capabilities.

The presentation will cover outline of highly integrated flow developed by Cadence and qualified by TSMC. Two sub-flows will be discussed in detail:

- Due to increased device complexity and its parasitics a new innovative method is required to better predict design performance in pre-layout stage and ensure correlation with post-layout simulation results. Macro Device approach, minimally disturbing existing schematic driven use model will be presented.

- Automated flow enabling designers to analyze LDE impact prior to layout completion, guide correct-by-construction layout and accurately identify and fix any LDE hotspots during layout and signoff.

The session will conclude with a real case study based on test chip designed by the Cadence IP team.



Addressing Custom Design Challenges for IP Design at 16nm FinFET technology

Jim McMahon, Product Engineering Director
Larry Aschliman, Sr. Design Engineering Manager

Cadence Design Systems, Inc.

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Outline

- 16nm FinFET Design Challenges
- Flow Overview
- New Tool Features
- Key Sub-Flows
 - Layout Dependent (LDE) Effects Sub-Flow
 - Parasitic Aware Design Sub-Flow
- Case Study

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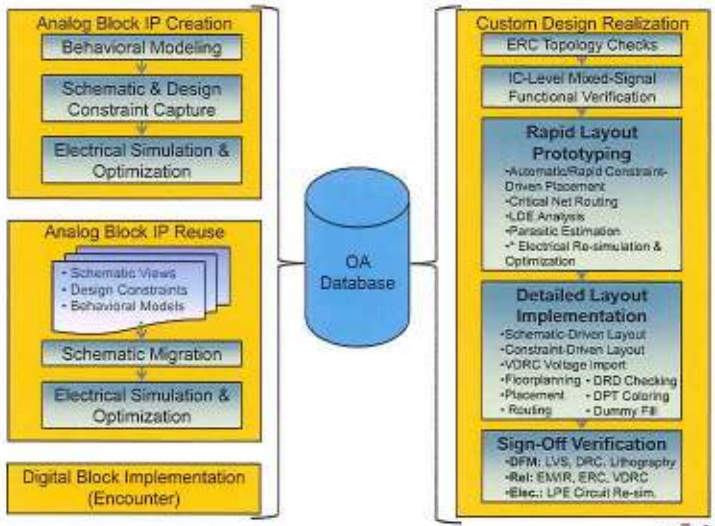
16nm FinFET Design Challenges

- Parasitics
 - Extracted device parasitics are more than 2x planar process
 - Device and interconnect parasitics have a larger impact on circuit performance
- Density Requirements and DRC Rule Complexity
 - Base layer density rules and guidelines for analog circuit matching
 - Complex design rules can be difficult to meet
- Layout Dependent Effects (LDE)
 - With smaller geometries, devices are closer to surrounding circuitry and the influences on device performance increase
- ESD and Electromigration (EM)
 - Thinner oxide makes devices more fragile and FinFET based ESD protection structures are larger in area
 - EM rules are increasingly complex
- Double Patterning
 - New challenges in layout stem from the extra patterning rules

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16nm Flow Overview
Cadence Schematic-Driven Flow

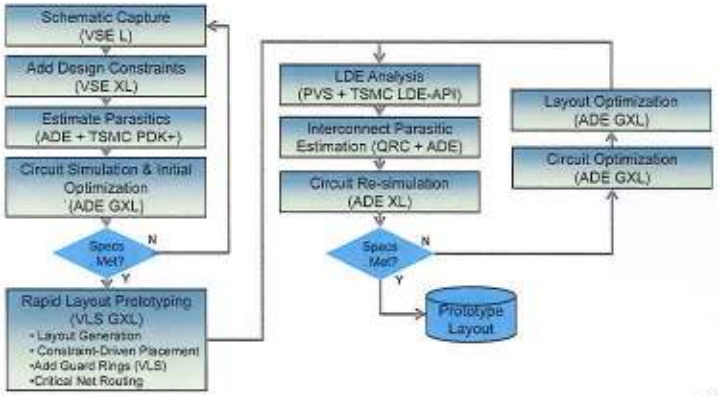


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16nm Flow Overview
Virtuoso Rapid Custom Block Prototyping

- **Goal:** Consider layout electrical performance impact early as possible in the design circuit optimization flow

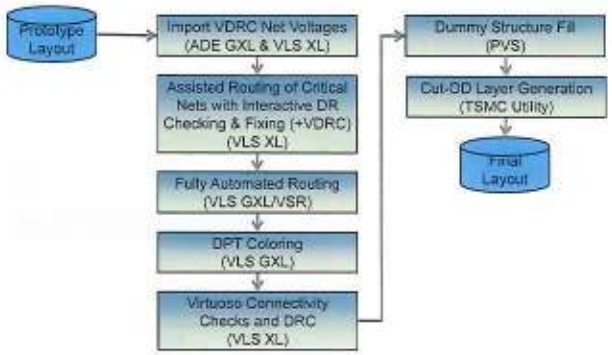


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16nm Flow Overview
Detailed Layout Implementation Flow

- **Goal**: Layout refinement and finishing with minimal impact on electrical performance

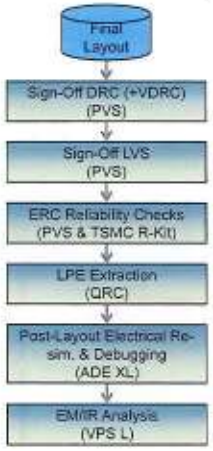


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16nm Flow Overview
Sign-Off Verification

- **Goal**: A manufacturable and reliable design meeting specifications

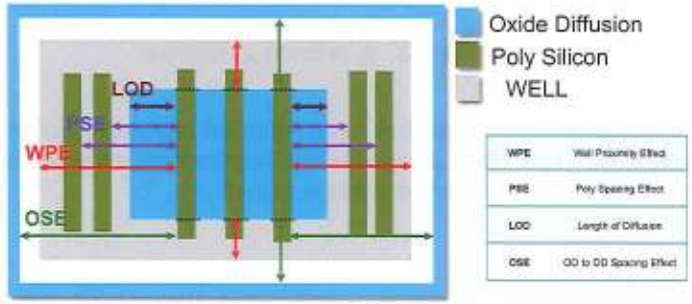


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Layout Dependent Effects
What are they? Why do they matter?

- **LDE** is the influence of the neighboring environment to the electrical performance of a transistor many different physical effects STI stress (LOD), WPE, PSE,… all combined into LDE
- LDE can significantly impact the performance of a device

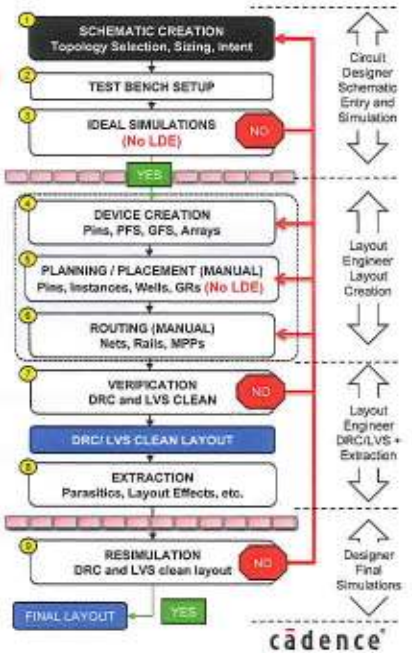


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Traditional Design Flow
Limitations at Advanced Nodes

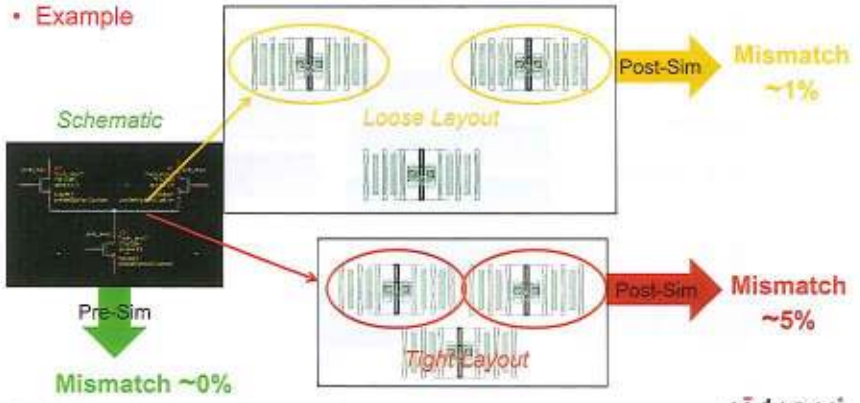
- All or nothing – no *incremental analysis*
- Issues detected *very late* in the design process
- Physical effects not *brought upfront* during circuit design
- Time consuming *serialized methodology*
- "Over the wall"



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LDE Affects Mismatch

- Different layout floorplan and spacing can give rise to electrical mismatch from LDE
- LDE may cause a large mismatch between the pre- and post-layout simulations requiring multiple design iterations
- Example



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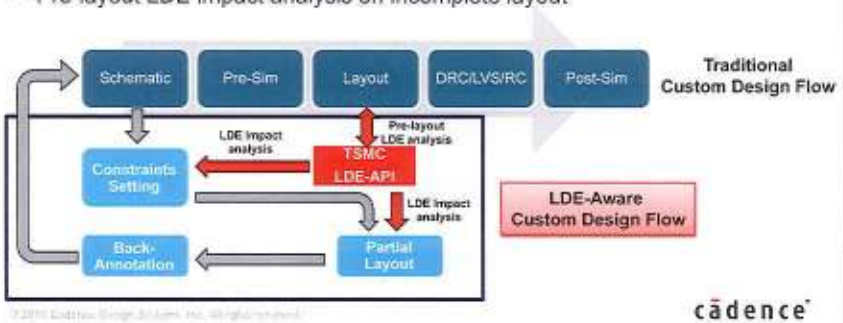
TSMC-Cadence Collaboration Enables In-Design LDE Analysis

- TSMC and Cadence jointly developed a new integrated LDE-aware custom design flow to minimize LDE impacts
- The LDE-aware design flow helps circuit & layout designers in:
 - LDE-aware re-simulation using device parameters from partial or completed layout
 - LDE analysis on pre-layout, with fixing guidelines
- The LDE-aware design flow has been validated and deployed for TSMC 28nmm 20nm, and 16nm processes and has become an essential in-design flow to reduce iterative loops at signoff

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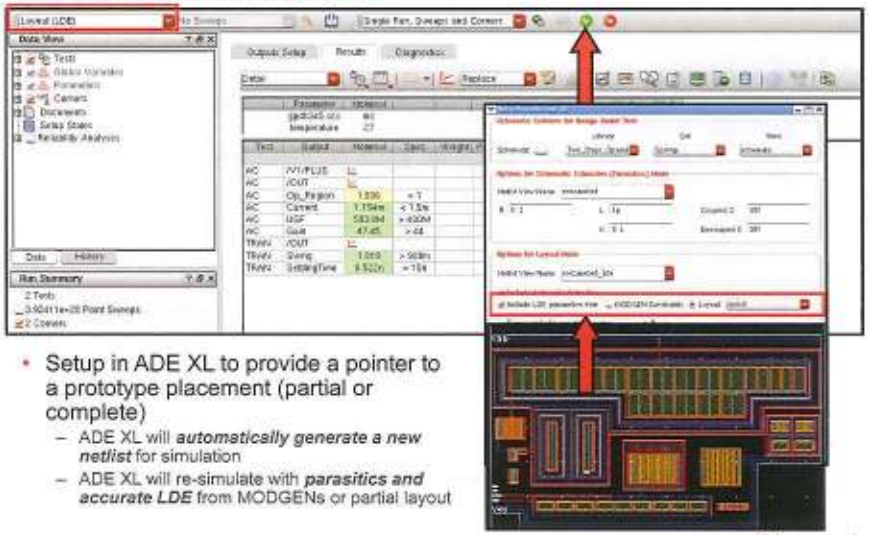
LDE-Aware Custom Design Flow

- TSMC's innovation of LDE-API with direct link to Cadence LDE Analyzer helps LDE analysis in both circuit design & layout
 - LDE analysis in schematic for constraints setting
 - LDE parameter extraction and simulation from partial or full layout
 - Back-annotate and compare LDE constraints for fixing
 - Pre-layout LDE impact analysis on incomplete layout



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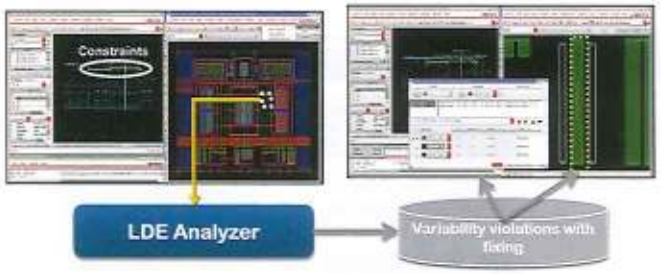
Layout Dependent Effects Simulation
Re-Simulation in ADE XL



- Setup in ADE XL to provide a pointer to a prototype placement (partial or complete)
 - ADE XL will ***automatically generate a new netlist*** for simulation
 - ADE XL will re-simulate with ***parasitics and accurate LDE*** from MODGENs or partial layout

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Layout Dependent Effects in Layout



- LDE analysis provides early detection and eases fixing of devices with large variability
 - Flags transistors with excessive variation in Idsat/Vth etc due to LDE
 - Works on incomplete layout (only transistor layers)
 - Typically reduces number of iterations by 2X
- LDE analysis verifies that the layout meets intended LDE matching constraints at layout stage

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TSMC LDE-API Customer Benefits

- Reduce design iterations by minimizing pre-sim & post-sim gaps through extracted LDE parameters from partial or full layouts
- Assist designers in analyzing LDE impacts to electrical performance using TSMC's LDE-API
- Facilitate back-annotation design flow for LDE parameters from layout to schematic through the built-in to TSMC PDK
- Seamless integration with Cadence design platform, simulation, layout and extraction tools

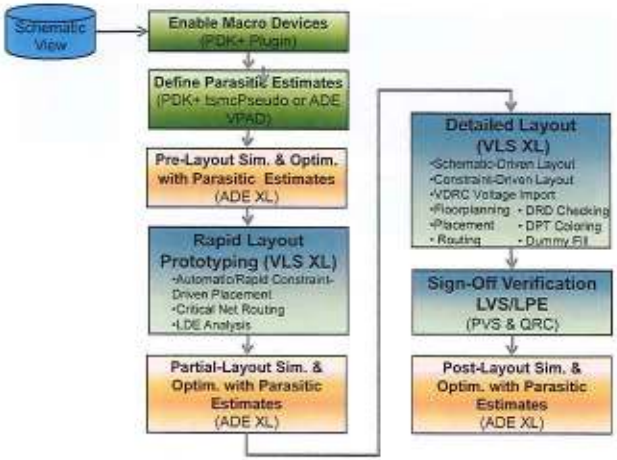
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Parasitic Aware Design Flow
Overview

- Challenges
 - Extracted device parasitics are more than 2x planar process
 - Device and interconnect parasitics have a larger impact on circuit performance
- Solutions
 - TSMC Macro Device Plugin =>Device-Level MEOL Parasitics
 - Cadence VPAD (ADE) Parasitic Estimation => Basic R/L/C/K BEOL Parasitic Estimates
 - TSMC Pseudo Parasitic Device Library => Complex BEOL Parasitic Modeling/Estimation
 - Any combination of these solutions can be used

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Parasitic Aware Design Flow



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Parasitic Aware Design Flow
TSMC Macro Device Plugin

- Methodology:
 - Select schematic PDK device instances requiring accurate MEOL parasitic modeling
 - Edit properties and set the **Model Type** parameter to ***Macro Device***



 - Some additional parameters will appear for including the PODE Effects



- Prerequisites:
 - Macro Device Plugin required => Available from PDK+ TSMC-supplied package

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Parasitic Aware Design Flow
ADE VPAD Flow for BEOL Parasitics

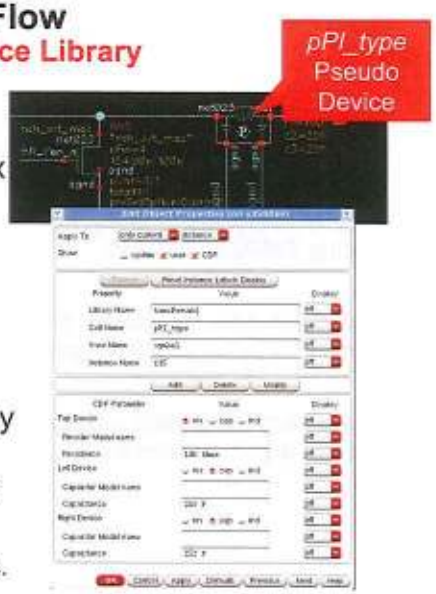
- **Enter virtual estimated parasitics without editing the schematic:**
 - **R/L/C/K parasitic device support**
 - **Stitch in parasitics from an existing layout**



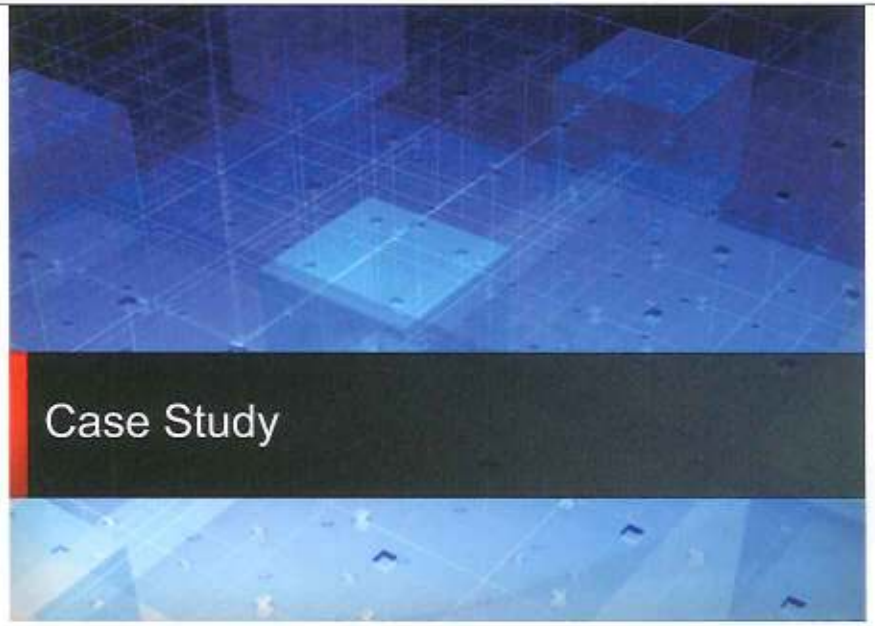
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Parasitic Aware Design Flow
TSMC Pseudo Parasitic Device Library

- Same purpose as VPAD but with support of more complex networks
- Library contains devices of "PI", "T", parallel, series, subcircuit, and S-parameter parasitic models
- Unlike VPAD flow, parasitic devices must be wired directly into the schematic view
 - Devices implemented to be fully compatible with the layout implementation (e.g. Cadence VLS) or sign-off (e.g. LVS) flows.



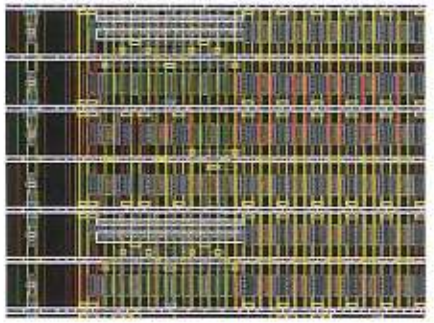
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Density and Design Rules

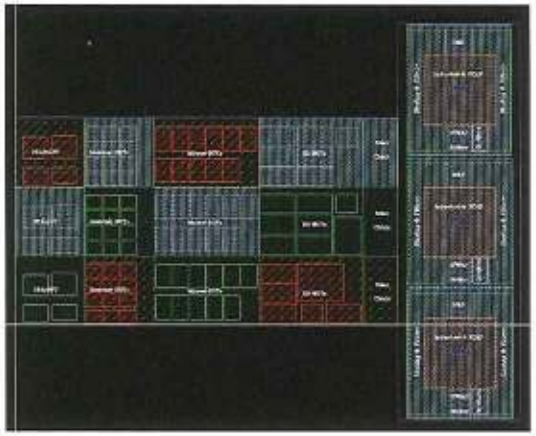
- Regular Design Style
 - Using a row based layout style keeps regular absolute and relative density for devices, improving matching
 - Device sizes are limited to fit into a standardized row height
 - Circuit Designers attempt to use a limited set of FinFET lengths to keep a common pitch where possible



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Test Structures for Shuttle Run

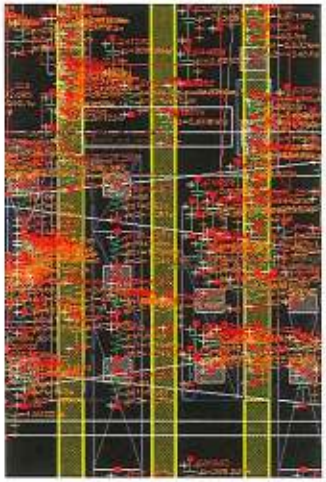
- Schematic Pcell views added to PDK



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Circuit Parasitic Extraction

28nm



16nm FinFET



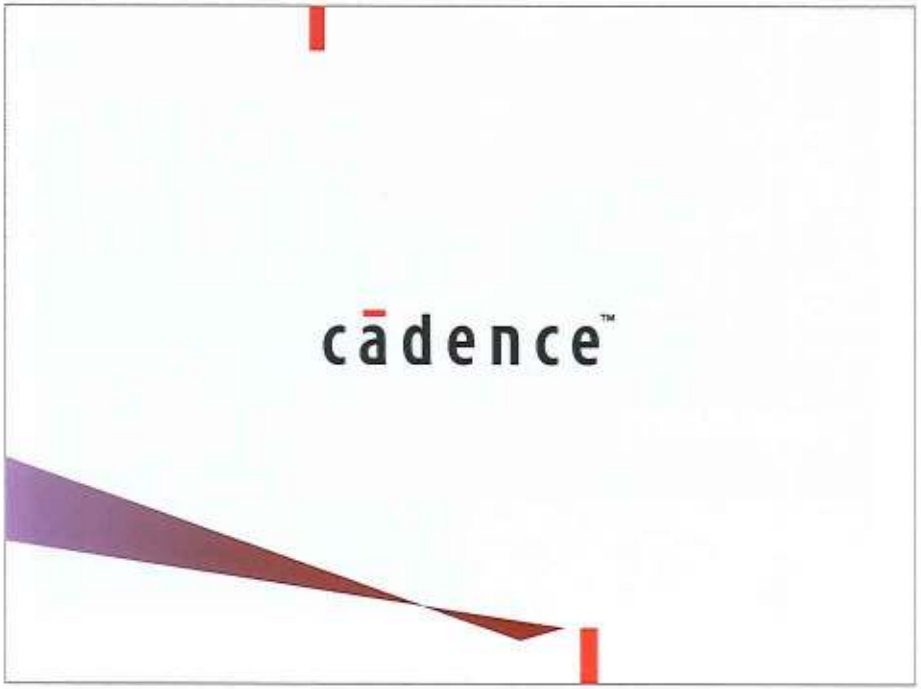
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Summary

- Cadence and TSMC have developed a complete design flow addressing all of the new 16nm FinFET design challenges
- A reference design database, presentations for key sub-flows, and associated tutorials is available for download from the TSMC Online web site. Covered sub-flows include:
 - Design Migration
 - Parasitic-Aware Design
 - Mixed-Signal Simulation
 - Analog Block Layout Implementation
 - LDE Aware Design
 - Variability Aware Design
 - EM/IR
 - VDRC
 - Reliability Analysis

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NOTE

A Synergetic, Multi-Partner, Soft Error Rate Analysis Framework for Latest Process Nodes

iROC

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

Perturbations induced by Single Event Effects (SEEs) may cause system downtime, data corruption and maintenance incidents. Thus, the SEEs are a threat to the overall system reliability performance causing engineers to be increasingly concerned about the analysis and the mitigation of radiation-induced failures, even for commercial systems performing in a natural working environment.

The SEEs are physical phenomena, strongly dependent on technological process and design implementation. Any realistic analysis attempt will absolutely require information, support and collaboration of TSMC as the technology provider. On the other end of the spectrum, any SEEs-induced faults have a potential for causing system-wide consequences, requiring a careful analysis and budgeting. Thus, any Soft Error Rate (SER) analysis approach will require a multitude of competencies. The reliability engineer will have to interact with all the actors from the design flow from TSMC to the system architect, while taking into account the reliability targets that are required by the final application or user.

We will present a short overview of a comprehensive SER analysis flow that can be used to evaluate and improve the overall SER reliability metrics of complex devices. The primary goals of the SER analysis are multiple:

First, the reliability engineer is able to characterize and document the reliability figures of the design in order to prove that stringent customer-driven expectations are successfully met.

Second, the application-specific SER figures of the design are evaluated, particular weaknesses identified and lower performances are highlighted for further refinement and improvement. Several optimization scenarios are supported by our tools, such as the use of TSMC-provided hardened cells and libraries.

Third, the design flow-oriented methodology allows the reliability and design engineers to share a common goal and use the same concepts and tools, across the TSMC's ecosystem.

Finally, the outcomes of the analysis help the reliability engineer choose the optimal error handling methodology in order to meet harsh reliability constraints, to ensure adequate data protection, to respect pre-defined system up-time constraints and to provide support and maintenance to the final user during the lifetime of the product. Moreover, the methodology provides early results that can be used in improving the circuit SER resilience through architectural and design choices with the firm goal of improving customer experience when using high availability products manufactured by TSMC.

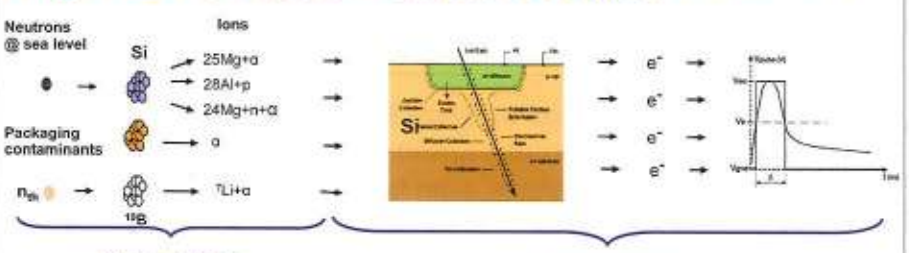
TSMC Open Innovation Platform Ecosystem Forum

A Synergetic, Multi-Partner, Soft Error Rate Analysis Framework for Latest Nodes

- Single Event Effects Overview
- SEEs – a Component of the System Reliability
- Exchanges and Actors Through the Flow
- A Standard SER Analysis Flow
- TFIT and SoCFIT Tools
- Examples of Multi-Partner SER Efforts

Dan Alexandrescu dan@iroctech.com
Olivier Lauzeral oil@iroctech.com

Single Event Effects – Global Overview



- Single Event Effects (SEEs) at ground level are caused by energetic particles from:
 - External sources: natural atmospheric neutrons
 - Internal sources: alpha particles from package contaminants
- Common manifestations: SEU (Upset), SET (Transient), SEL (Latch-up), SEFI (Functional Interrupt)

SEE: A challenging aspect of overall system reliability

- SER knowledge applicable to problems coming with nanometric technologies:
- Process, voltage and temperature variations, cross talk, timing faults, ageing

SEEs – Why Should I Care?

- **Usual fields:** Aero-space applications
 - A satellite was launched from Baikonor Cosmodrome, Kazakhstan on 31 May 2005
 - Failed during the 5th orbit instead of after a total of 253 orbits (2% use)

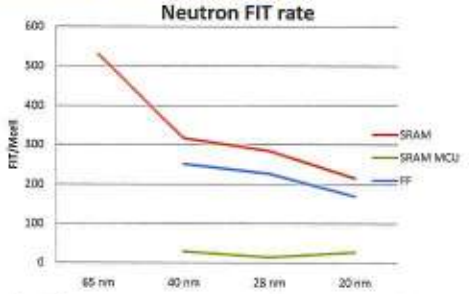




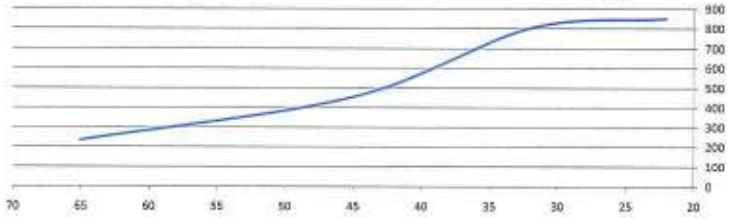
Source: Rene Harboe-Sorensen, ESA-ESTEC, " Radiation Effects in Spacecraft Electronics", 5th LHC Radiation Workshop –Nov-29, 2005

 - A latch-up condition in a SRAM was concluded as the possible cause
- **SEEs:** Coming down to earth
 - **1970's:** First studies on SRAM susceptibility to alpha particles… and still many years later:
 - **2000's:** Alpha problems in CPU cache memories (used in high-reliability servers)
 - **Elections** in Belgium: electronic voting machines on **05/18/2003** (Schaerbeek):
 - More votes compared to number of registered persons: shift of … 4096 votes !
 - A SEU effect on 13th bit in SRAM was considered as the possible causes
 - **Now:** Atmospheric neutrons, low energy protons, multi-cell errors, transients, X-rays dose effects in DRAMs

SER Observations (from IROC)



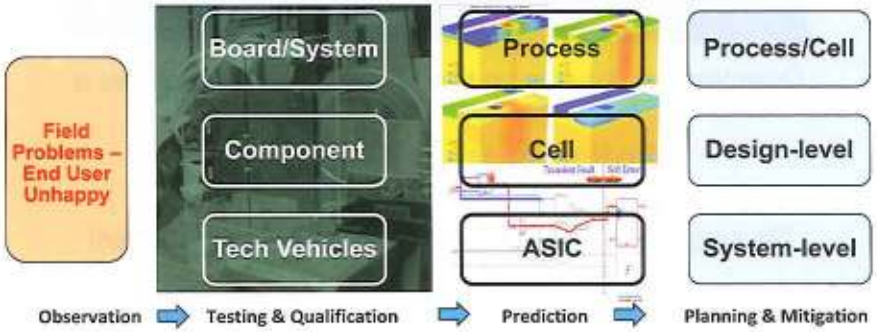
Total FIT (Processor, ECC protection, structural derating)



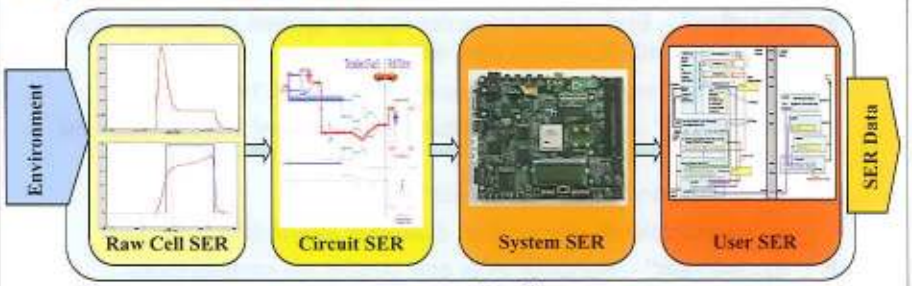
SEEs – Life Cycle



A progressive shift of focus and responsibilities:



A Systematic Approach

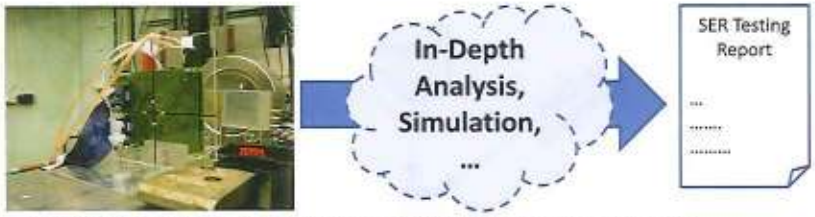


- **Methodology**
 - Breakdown the full SER analysis flow to stand-alone tasks
 - Each module is tackled by appropriate tools (or engineers)
 - Tasks to be performed as early as possible in the design flow
 - Use standardized SER data(bases)
 - Based on gained experience, elaborate dedicated tools to supplement expertise
- **Benefits**
 - Standard, unified approach
 - Common SER metric
 - Centralized SE expertise made available to "normal" user
 - Growing database of library/process characterisation data, circuit & application profiles
 - Early SER analysis during the design flow
 - Encourages "best practice" scenarios

IOLTS 2008: "Systematical Method of Quantifying SEU FIT", *S. Wen, D. Alexandrescu*

Earlier Multi-Partner SER Efforts

- **"We want SER data!"**



- System Integrators may request SER data concerning ICs
- Offering selection (product, supplier) have been observed
- Memory devices well known and specified (procedures, data)
- Other more complex devices: ???
- Gradual evolution towards consistent SER testing procedures:
 - Environment: neutrons, alpha (commercial, ground apps)
 - Observed Events: definition, statistics
 - Testing Procedures: same across vendors, etc

Current Multi-Partner SER Efforts

- **"We expect good SER behaviour!"**



- SER expectations & requirements concerning ICs, IPs, etc
- A more pro-active role for all design flow partners
 - Technology providers (foundries): support SER analysis through technology specific SER data (ex: TFIT databases)
 - IP/IC providers: SER data, recommendations
 - SER Solutions providers: SEE tools and services for improving overall design reliability

An absolute need for common terminology, definitions, specifications, ...

Reliability Eras

- **"Reactive"** – End users encounter issues, system integrators and solutions providers have to deal with them
 - Product recalls, hardware updates, software hot-fixes, …
- **"Awareness"** – System integrators pre-emptively acknowledge the issue
 - System and component-level testing
 - Specifications, procedures, customer interaction …
- **"Exchanges"** – Requirements and targets are progressively propagated in the supply chain
 - SER targets for components, SoCs, ASICs, systems
 - Technology, IP, materials, suppliers selection
- "**Proactive**" – Objective requirements will drive the design and manufacturing flow towards SER management and optimisation
 - Process, IP, design, system-level SER optimisation
 - Design and manufacturing recommendations, constraints, ...

Soft Error Rate Analysis Synergies



Sub-Atomic Event → Charge Deposited → Cell Upset → Complex Circuit Impact → System Impact

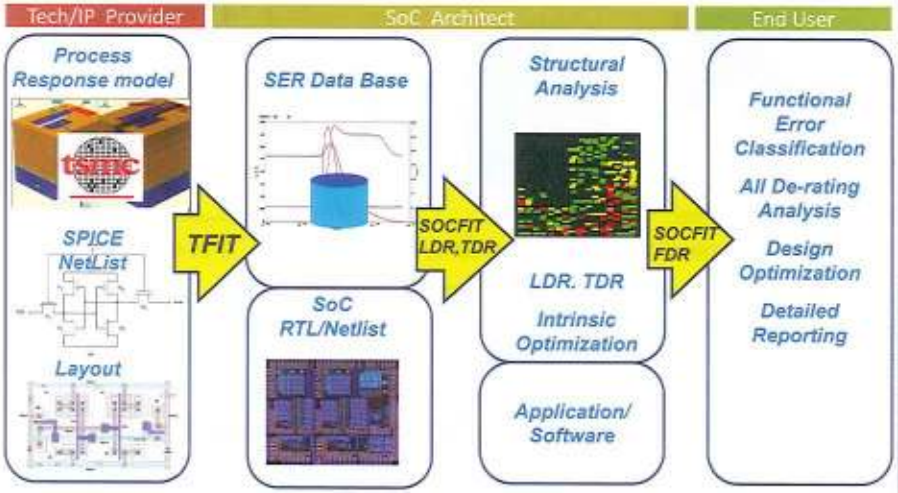
Quantitatively analyzing this chain of events requires a

Collaborative Approach

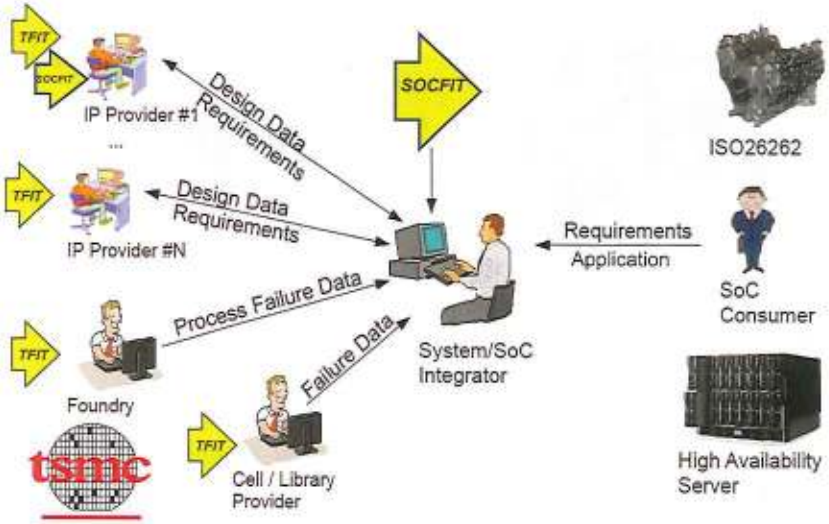
No single organization has the end-to-end expertise!

TSMC and IROC have a strong partnership to provide solutions!

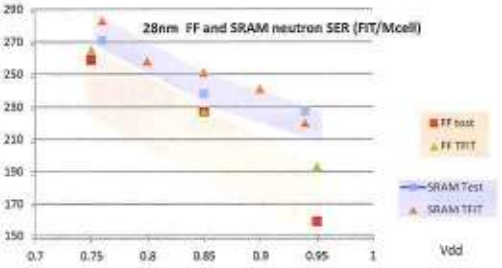
SER Analysis/Prediction Platform



SoC Reliability Analysis Collaboration

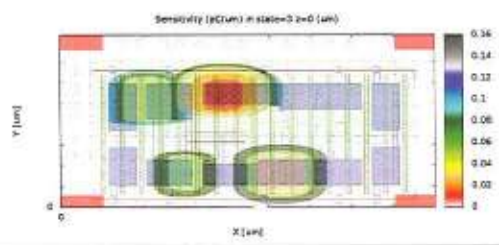


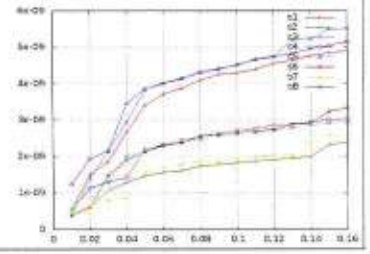
Cell FIT Rate Prediction Tool: TFIT®



Process models developed with TSMC, calibrated with TSMC's test chips results

- 40 G DNW
- 28 HP DNW & nDNW
- 28 HPM nDNW
- 20 SOC
- 20G





Accurate De-rating Analysis Critical



Example

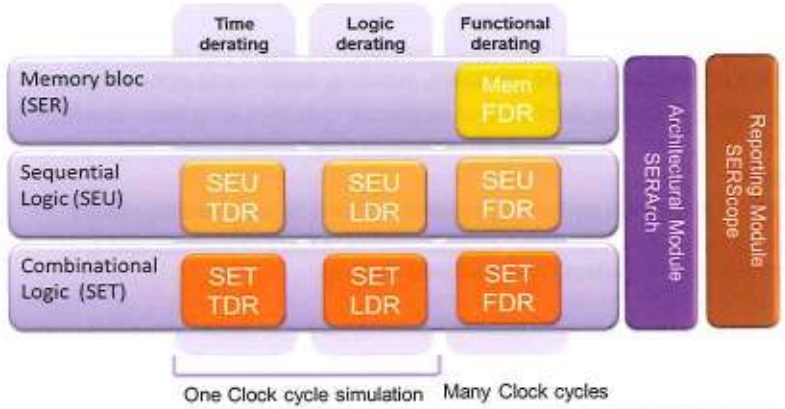
			Fit by Effect
1000 FIT (raw)	LDR : 0.2 TDR : 0.8	160 FIT (derated)	SDC : 20 FIT DUE : 140 FIT

- Not all SEEs manifest themselves as faults
- Derating factors are significant (often only 1%..10% of SEUs have an observable effect)
- SOCFIT accurately calculates derating factors

Chip SER Failure Rate Prediction

SOCFIT tool: circuit FIT prediction and de-rating analysis tool

External requirements: timing analysis or synthesis tool access (SEU TDR)
SER DB needed for the technology (built with TFIT or test), simulation tool



A SER-Aware ASIC Design Flow



Multi-Partner SER Efforts (I)

- **IEEE TNS (December 2009), 56 (6, 1), pg. 3551-3555:** "Design for Soft Error Resiliency in Internet Core Routers", *A. L. Silburt, A. Evans, I. Perryman, S. Wen, D. Alexandrescu*
- **SER actors:** Cisco/IROC
- **Devices Under Test – Core Internet Routers**
 - Extensive error mitigation features
 - Migration to a new process
- **Benefits**
 - Accent on specifying SER performance of the circuit as a part of the system reliability, fulfilling tough reliability expectations
 - Sequential (SEU) Temporal & Functional De-rating for accurate functional SER data
 - Optimised Hardened Flip-Flop instances Selection for reduced overheads: design, power & silicon costs

Multi-Partner SER Efforts (II)

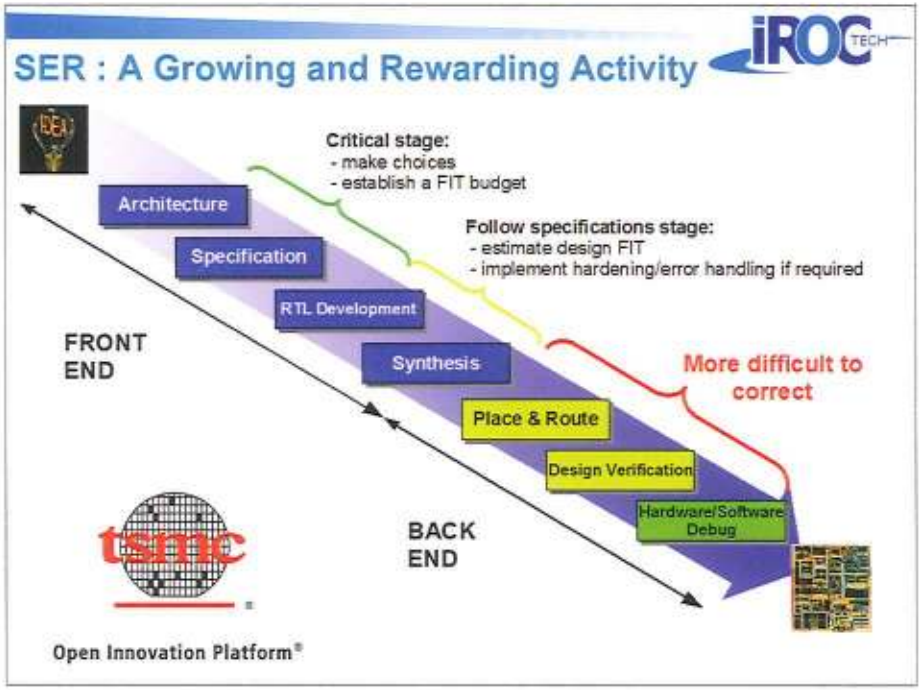
- **SELSE 2010:** "A Multi-Partner Soft Error Rate Analysis of an InfiniBand Host Channel Adapter", *H. Chapman et all*
- **Typical SER actors:** Mellanox/TSMC/IROC
- **Device Under Test - Host Channel Adapter (HCA)**
 - Existing design (90nm); utilisation example: 4000-node system
 - Extensive error mitigation features
 - Field data available & very satisfactory
- **SER Methodology**
 - Cell SER characterisation through the TFIT tool
 - Memory (SBU/MCU/MBU), Sequential (SEU) & Combinational (SET) cells analysis, including error mitigation efficiency analysis - SoCFIT
 - Logic, temporal & functional de-rating on RTL & Netlist design views - SoCFIT
- **Benefits**
 - SER methodology can be easily integrated in the standard design flow
 - Multi-partner collaboration works
 - Results proven quality and reliability

Multi-Partner SER Efforts (III)

- **IOLTS 2012:** "A Real-Case Application of a Synergetic Design-Flow-Oriented SER Analysis", *Miguel Vilchis, Ramnath Venkatraman, Enrico Costenaro, Dan Alexandrescu*
- **Typical SER actors represented:** LSI/IROC
- **Device Under Test - TPV: Test Chip on Power & Variation**
 - Advanced Encryption Standard (AES) blocks
 - Each PE: 50K cell instances of which 3.3 K are standard flip-flops
 - Up to 500 MHz operation
- **SER Methodology**
 - Cell SER characterisation through the TFIT tool
 - Sequential (SEU) & Combinational (SET) cells analysis thru SoCFIT
 - Alpha radiation testing approach
- **Benefits**
 - Early, TFIT+SoCFIT SER data correlates very well to actual radiation testing results
 - Evaluate, improve circuit SER resilience thru architectural & design choices

Multi-Partner SER Efforts (IV)

- **SELSE 2013:** "Neutron and Alpha Soft Error Rate Simulations for Memory and Logic Devices at Advanced Technologies", *Yi-Pin Fang (TSMC), Anthony S. Oates (TSMC), Kader Belhaddad (IROC), Vincent Correas (IROC), Issam Nofal (IROC) and Olivier Lauzeral (IROC)*
- **Typical SER actors:** TSMC/IROC
- **Results**
 - Complete, exhaustive, TFIT characterisation of single and multiple bit errors in advanced SRAM memories, including neutron and alpha results
 - Single Event analysis of several sequential cells, including state-specific data
- **Benefits**
 - TFIT SER data is perfectly correlated to actual radiation testing results
 - TFIT simulation is an early, detailed approach to SER analysis and a complement and alternative to radiation testing


SER : A Growing and Rewarding Activity
iROC TECH
Critical stage:
- make choices
- establish a FIT budget
Follow specifications stage:
- estimate design FIT
- implement hardening/error handling if required
Architecture
Specification
RTL Development
Synthesis
Place & Route
Design Verification
Hardware/Software Debug
FRONT END
BACK END
More difficult to correct
tsmc
Open Innovation Platform®

EDA-Based DFT for 3D-IC Applications

Mentor Graphics

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ABSTRACT

Testing of TSMC's 2.5D/3D ICs implies slight changes to traditional Built-In Self-Test (BIST) insertion flows provided by commercial EDA tools. DRAMs (e.g. Wide-IO) are put on separate dice – so their Verilog model is not part of the design used during DFT insertion. Since those memories are externally accessed, a robust method is required to test them, potentially at any point during the stacking process – i.e. before, during and/or after assembly. BIST being "vendor-independent", a second-source memory may even be used. Gross defects in the logic die IOs and/or interconnects are also verified, using a time-proven IEEE 1149.1-based contactless test access method.

Gross IO and interconnect defects are identified as soon as possible in the production test flow, by executing contactless tests resulting from the use of "IO wrap" (i.e. bidirectional boundary-scan cells added to the design IOs). To test a stand-alone bare die, an input/output test is applied to functional IOs via the JTAG interface. This requires the ATE to contact only the 5 (optionally 4) mandatory TAP pins. Using boundary-scan, steady-state 0 and 1 values are applied to the die pads/pins output buffers – and are then captured back via the input buffers of the same IOs. Pins/pads that are stuck-at, bridged or open are thus detected early, before 2.5D/3D assembly takes place – so only IO-tested dice are stacked.

The same test infrastructure is used to perform a contactless leakage test – e.g. to detect blown ESD protection diodes on IOs. Pins, pads or even TSVs are first driven to 1 and then tri-stated. The logic 1 value will start to decay due to leakage current; the IO pin logic state is captured after a precise (and specific) number of TCK clock cycles. Higher-than-expected leakage currents make the IO pad voltage decay faster, resulting in the opposite values being captured. The test is repeated with opposite apply/expect values.

Once stacked, interconnects between the logic and memory dice (whether TSVs or traces) are also verified with a contactless method. Standard boundary-scan patterns are generated using IEEE P1687 – also known as IJTAG. These test patterns ensure interconnects are at least capable of driving/capturing steady-state values across dice. A very quick and early detection of easily-diagnosable interconnect faults is achieved without having to wait for the next step results.

Finally, memory BIST is run on the external Wide-IO DRAM, allowing a true at-speed test to be carried on. Unlike with embedded SRAMs, there are no compiler-generated memory models to drive BIST generation and insertion; the model is thus created based on the design-specific connectivity. Memory operations (such as basic reads and writes) are first predefined and then used algorithmically, allowing the implementation of both standard and custom test algorithms. The memory BIST controller allows "soft" algorithm recoding, so test algorithms can be created (or modified) after silicon has been manufactured. This allows fine-tuning the implemented BIST algorithm(s) after newer defects have been root-caused, thus reducing expensive design iterations or ECOs and ultimately translating to a lower cost per device.



EDA-Based DFT for 3D-IC Applications

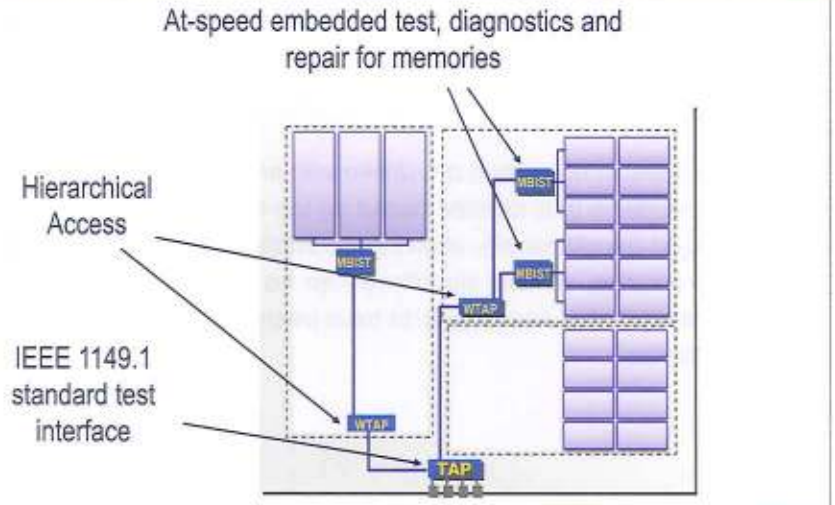
Etienne Racine
Mentor Graphics

EDA Challenges & Requirements

- DRAM not within DFT design
- DRAM may be second-source
- Gross defects in I/Os must be detected
- Perform contactless I/O tests (+leakage)
- Need interconnect tests across dice
- Memory BIST is very design-specific
- Run-time programmable MBIST is essential for yield

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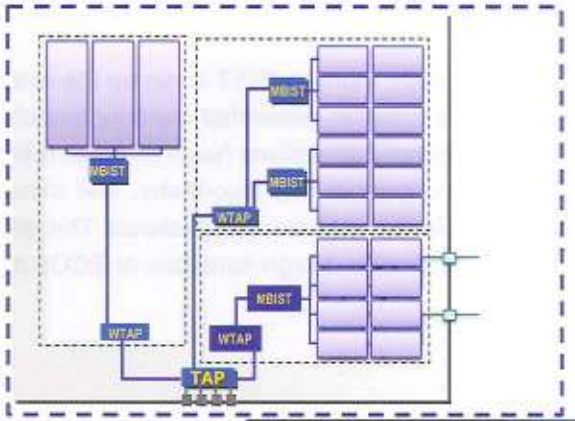
Typical DFT for Embedded SRAMs



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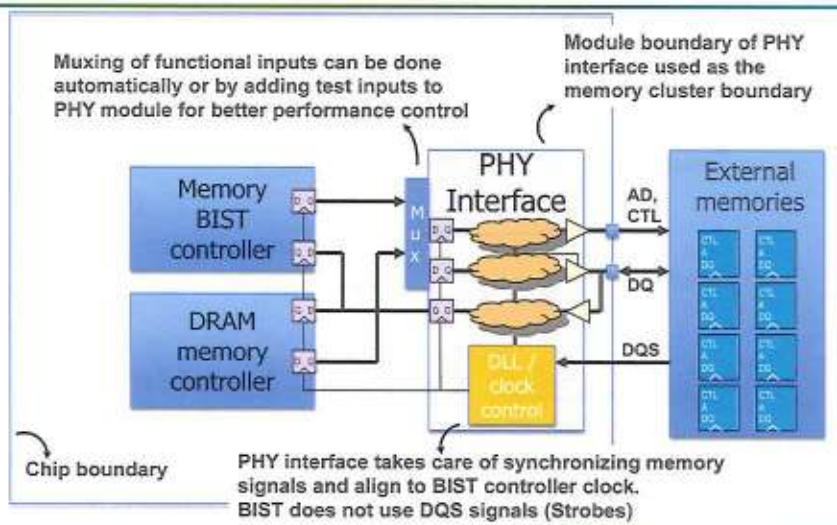
Memories No Longer Visible to DFT

- SRAMs already within design during DFT insertion
- DRAM (e.g. Wide-IO) instantiated outside of design
- Indirect access through Physical Interface (PHY)
- BIST now applied to PHY interface
- Need wrapper & DRAM, IO models for simulations



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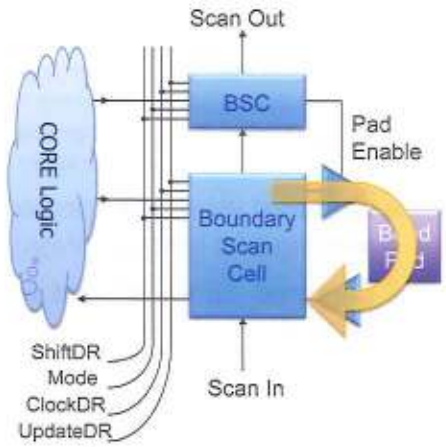
BIST Interface to External Memories



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Contactless I/O Testing via Boundary Scan

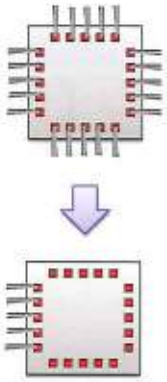
- Uses bidirectional I/Os + boundary scan cells
 - a.k.a. "IO-Wrap"
 - Supports bidirectional or separate in/out BSCs
- Output BSC drives 0/1, captured by input BSC
 - Shifted-out for comparison
 - ATE can optionally monitor
- Tests Output Enable path
 - Drives output to 0
 - Tristate I/O pad & apply 1
 - Capture logic 0 on input
 - Repeat with opposite value



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Identifying I/O Defects

- Bare die verified early on
 - ATPG, BIST, TAP tests, etc.
- Must also detect driver/pad defects
 - Including Through-Silicon Vias (TSVs)
- EDA generates I/O test patterns
 - Reuse IEEE 1149.1/.6 logic on chip
- Use ATE resources on contacted I/Os
 - Inputs: Capture test, measurement of I_{IL} & I_{IH}
 - Outputs: Update test, measurement of V_{OL}, V_{OH}
- → Also test non-contacted I/Os
 - Fewer tester channels/resources per die
 - Increases # of dice tested in parallel
 - Reduces probe-induced deterioration



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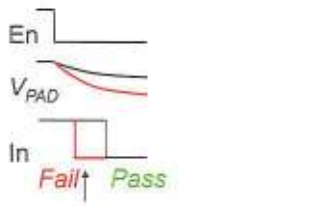
3D-IC Implications on Memory BIST

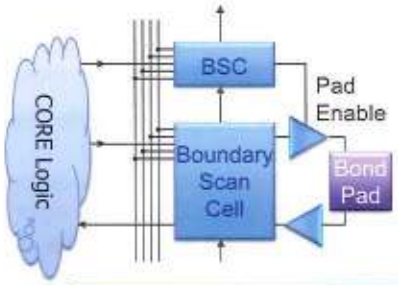
- BIST is memory vendor-independent
- Yet DRAM die may be second-sourced
 - i.e. similar specs but different vendor
- Memory array topology differences
 - Checkerboard background no longer guaranteed
 - **Potential** impact on BIST quality & yield
- Architecture, specs change over time
 - i.e. increase in memory depth, max. frequency, etc.
 - Implications on DRAM-specific commands (operations)
- → EDA implements **flexible** memory BIST solution
 - Various background patterns, multiple address spaces
 - Implement & select among different operation sets
 - Modify test algorithms used by BIST **even post-silicon**

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Contactless I/O Leakage Test

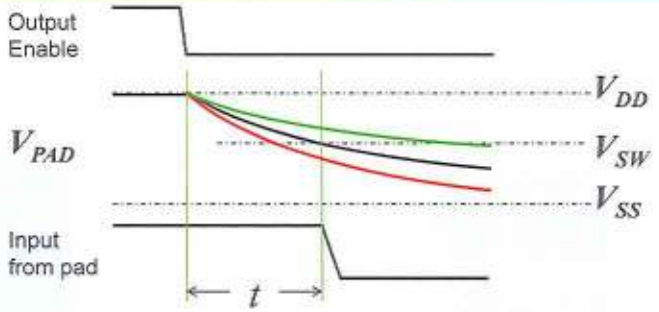
- Similar to Output Enable test
 - Pad is first pre-charged to 0/1
 - Pad is then tristated, charge decays w/ leakage current I_{LEAK}
 - Pad value is captured precisely <N> TCK clock cycles later
- Captured value as expected with normal leakage (Pass)
- Captured value different with excessive leakage (Fail)
- N is variable & either derived from characterization data or calculated from std. equation





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Contactless I/O Leakage Tests Details



$$t \approx \frac{C_{PAD}\,(V_{DD} - V_{SW})}{I_{LEAKAGE}} = \frac{3pF\,(3V - 1.5V)}{1\mu A} = 4.5\ \mu s$$

$t = C_{PAD} \times (-\ln(V_{SW}/V_{DD})) \times (V_{DD}/I_{LEAKAGE})$

Decay time — Switching voltage — Leak current

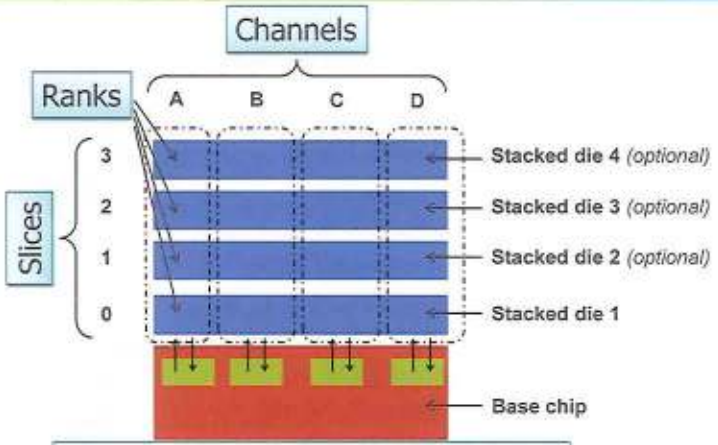
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Logic Die ⇔ DRAM Interconnect Tests

- Newer DRAM standards include boundary scan
 - Wide-IO, Wide-IO2, HBM, HMC, ...
- JEDEC boundary scan ≠ IEEE 1149.1
 - Often a simple serial shift register (e.g. Wide-IOx)
- TAP interface to JEDEC boundary scan
 - Custom glue logic inserted by EDA tools
- IEEE P1687 (IJTAG) language unites both standards
 - Generates tests for logic ⇔ memory interconnects
 - Exports Verilog TBs for simulation
 - Exports WGL, STIL or SVF patterns for test

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Wide-I/O Interconnect Tests

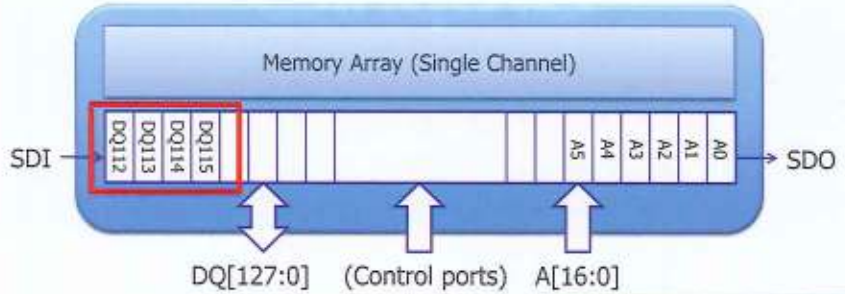


Channels across slices are fully independent
(i.e. separate CLK, ADDR, DATA & CTRL ports for each)

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Wide-I/O Interconnect Tests (.../2)

- 179-bit long scan register (one per channel)
 - — Out-of-order bit indexes (e.g. DQ[127:0], shown below)
 - — Die position-dependent bits (e.g. CS_n[3:0], CKE[3:0])
 - — Odd/even patterns insufficient – check across all bit pairs
- ➔ Interconnect test patterns account for the above



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Wide-I/O Interconnect Tests (.../3)

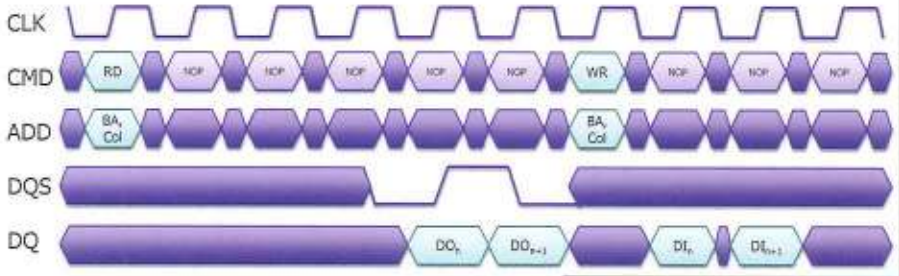
- Boundary scan register concatenated across all channels
 - — 4 x 179 bits = 716 bits
 - — Then connected to a standard 1149.1 TAP
- P1687 (IJTAG)-generated patterns
 - — 0101 0101 0101 ... 0101 0101 0101
 - — 0011 0011 0011 ... 0011 0011 0011
 - — 0000 1111 0000 ... 1111 0000 1111
 - — ...
 - — 1010 1010 1010 ... 1010 1010 1010
 - — 1100 1100 1100 ... 1100 1100 1100
 - — 1111 0000 1111 ... 0000 1111 0000
 - — ...

Test length ≈ $2*Log_2(N_{BITS})$

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Wide-I/O Example Waveforms

- Below waveforms for RL=3, WL=1 (at memory pins)
- PHY requires additional latency & retiming
 - — Not shown – but impacts waveforms
- Read/Write waveforms thus based on PHY
 - — Not on memory standards



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Wide-I/O BIST Operations

- Define basic DRAM waveforms ➔ Operations
 - — e.g. NoOp, Read, Write, ReadModifyWrite, ...
 - — One operation set per test mode settings
 - — Create as many variations as wanted
- Operation sets then selected at run time

```
OperationSet (WideIO) {
  PipeliningStages (Data)              : 1; // Same as WL value
  PipeliningStages (StrobeDataOut)     : 4; // Same as RL+1 value

Operation (Read_BL2) { // RD with Burst Length = 2
  Tick { RAS: Off; CAS: On;  StrobeDataOut:    Address: Column; ColumnAddressCount: On; }
  Tick {           CAS: Off; StrobeDataOut:    Address: Row;    ColumnAddressCount: Off;}
}
Operation (Read_BL4) { // RD with Burst Length = 4
  Tick { RAS: Off; CAS: On;  StrobeDataOut:    Address: Column; ColumnAddressCount: On; }
  Tick {           CAS: Off; StrobeDataOut;    Address: Row;    ColumnAddressCount: On; }
  Tick {           CAS: Off; StrobeDataOut;    Address: Row;    ColumnAddressCount: On; }
  Tick {           CAS: Off; StrobeDataOut;    Address: Row;    ColumnAddressCount: Off;}
}
```


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Conclusions

- EDA-based DFT for 3D-ICs is in place
 - Leverages time-proven access methods (IEEE 1149.1, IEEE 1500)
 - Needs customization based on design, flow
- Generates contactless I/O and interconnect tests
 - Prevents stacking defective dice
 - Performed early in the 3D stacking flow
 - Rely on IEEE P1687 (IJTAG)
- Implements advanced memory BIST for DRAM
 - Programmable memory operations
 - Run-time selection of waveforms
 - Post-silicon algorithm changes

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NOTE

Advanced Power, Signal and Reliability Verification for 20nm, 16nm FinFET, and 3D-IC Designs

ANSYS Apache

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

Chip designs using 3D-IC, silicon interposer-based or vertically stacked die designs with TSVs require advanced modeling, simulation and debug capabilities to meet the demands of low-power mobile, high-performance computing, and consumer and automotive electronics. However, there are challenges in meeting these demands including verification of power, signal and reliability integrity.

With the introduction of 16nm FinFET designs, a higher current-drive and lower voltage-operation contribute to power integrity and EM reliability issues. The addition of middle layers (below M1 and above device layer) in 20nm/16nm designs can further increase the complexity in power/signal EM checking. Another concern of 20nm/16nm reliability is the need for a comprehensive layout-based full-chip ESD check to address a narrowing safe ESD design window caused by lower oxide breakdown and operating voltages. With dramatic increase in the number of on-chip supply voltages in ultra-low-power designs, the complexity of ESD protection among inter-domains is growing and needs to be automatically checked. Employing a methodology flow that provides a verification platform for 20nm/16nm designs to meet the increasing complexity of power, signal, and reliability checking is key.

From a power integrity perspective, designing the PDN to multiple die becomes more challenging with TSVs, passing power from the die closer to the package on to the die higher in the stack. The use of TSVs can cause inter-die noise and other reliability issues. This paper proposes two methods, illustrated in two different design scenarios. First, a concurrent analysis approach, where layouts of the die including the Silicon Interposer are concurrently simulated; assuming all the die data is available. The second approach is a model-based analysis, where some die data is not available, for example from an IP vendor, so a CPM is generated for co-analysis with the core die(s).

Additionally, a power related problem exists with thermal failures of 3D-ICs in a system environment. This challenge is on the operation mode switchings in mobile devices, such as on smart phones from watching a movie to reading an e-mail, the thermal signature is very different and requires a transient thermal simulation for system reliability. It is also important to decide the locations of thermal sensor placement or maximum delta of temperature between the sensor and actual location where maximum temperature occurs. A fast dynamic thermal analysis is required to help predict the actual temperature on chips in a sequence of operation modes.

From the signal integrity perspective, a significant problem has surfaced on jitter noise analysis for wide-I/O applications on Silicon Interposer and vertically stacked die designs. The requirement to have simulation of more than one thousand bits within a reasonable amount of time also demands simulation technology innovation. Apache Design has developed the CIOM as a chip I/O macro-model for fast parallel bit simulation.

In summary, a comprehensive analysis methodology is required for power, signal, and reliability issues to ensure a timely and successful design tape-out.

ANSYS Apache

Realize Your Product Promise™

Advanced Power, Signal and Reliability Verification for 20nm, 16nm FinFET, and 3D-IC Designs

Fluid Dynamics | Structural Mechanics | Electromagnetics | Systems and Multiphysics

Norman Chang, VP & Sr. Product Strategist
TSMC OIP, Oct. 2013

Apache Design, a subsidiary of ANSYS

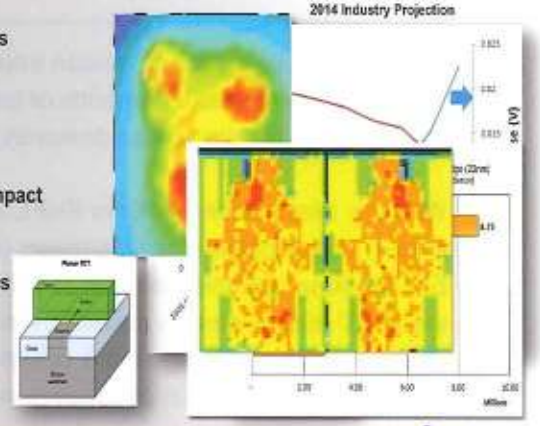
ANSYS Technology Trends and Challenges

Decreasing Nominal Voltages
→ Less Noise Margin

Increasing Gate Density
→ Elevated Thermal Impact

Higher Drive Strength Devices
→ Higher Ldidt noise

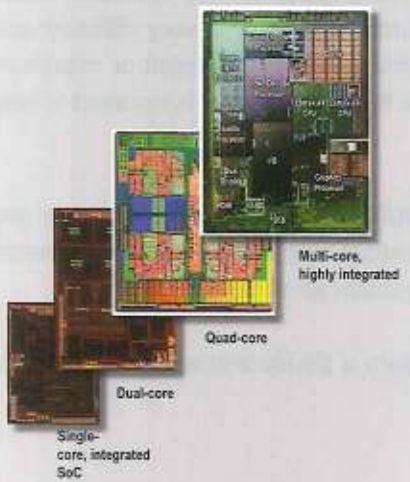
Shift from Planar to FinFET



65nm 40nm 28nm **20nm** **16nm**

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ANSYS Design Trends and Challenges



Scale Performance without Scaling Power
→ MHz/mW impact

Multi-core, Multi-threading
→ Higher throughput @ lower V, power

On-die Power Regulators
→ Reduce package/PCB impact

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ANSYS ANSYS-Apache Technologies for Power Noise Closure

RTL Design	**Design for *Power*** Manage power consumption early in the architecture phase	**PowerArtist** RTL power analysis, reduction, regression
Physical Design	**Design for *Performance*** De-risk increasingly complex power delivery network	**RedHawk/Totem** PDN integrity, advanced reliability sign-off
System Design	**Design for *Price*** Reduce total electronic system cost	**SentinelSiwave/ HFSS** Chip-aware system-level PI, SI, EMI, thermal

Apache Design, a subsidiary of ANSYS

EDA Collaboration Between TSMC and Apache

Anticipating and addressing upcoming design challenges associated with new processes

16nm Certification & 3D-IC Solution

- N16 R/IR/EM certification
- 3D-IC w/ TSV design
 - Dynamic thermal analysis and back-annotation for IR/EM
 - Global decap co-optimization for chip-package-system
 - SSN analysis with accurate TSV model extraction

Analog/Mixed-Signal

- Within cell power/signal EM qualification for 16nm
- ESD check on I/O, macro and SoC

Outline

- IR/EM Support for Emerging 20nm, 16nm FinFET
- ESD R and Current Density Check for Macro/SoC
- Power, Thermal and Signal Integrity for 3D-IC
- Summary

20nm/16nm Readiness

Support for Metal Stack

- Special metal layers for local interconnects
- Complex via structures and shapes
- Diffusion as via and local interconnect structures

Support for Device & RC Extraction

- Dummy device
- TMI model
- Vertical resistance
- Width and thickness bias on metals
- Double patterning

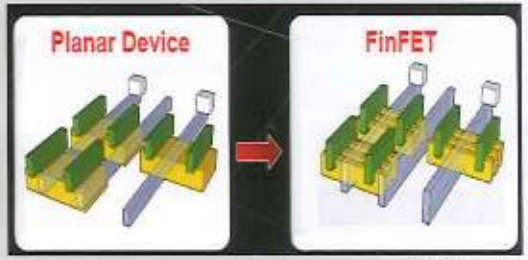
Support for EM Rules

- Current-direction, metal overlap aware
- Polynomial EM rule
- Width, temperature, self-heat and other parameter dependent EM
- Back-end /pseudo via RMS/Peak EM

20nm / 16nm Requirements

RedHawk and Totem Certification for IR/EM

- 20nm
 - Fully qualified in R, IR, and EM accuracy
 - Ready for customer usage
- 16nm FinFET
 - Resistance correlation including Middle-end and Back-end layers
 - EM Rule handling
 - Ready for early adopters



Courtesy of TSMC

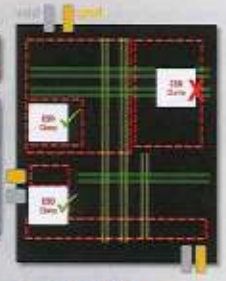
ANSYS Outline

- IR/EM Support for Emerging 20nm, 16nm FinFET
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ANSYS ESD Integrity Coverage

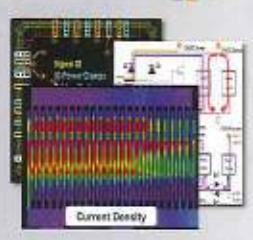
Floorplan

- Power grid prototyping
- Core clamp placement
- Grid connectivity checks

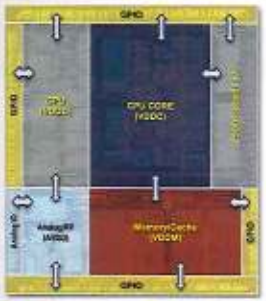


IP Level / I/O Ring

- ESD bus resistance checks
- Current density/IR checks
- IP-level transient simulation



Full-chip Sign-off



- Pin to Pin connectivity checks
- Cross-domain checks
- SoC-level current density checks

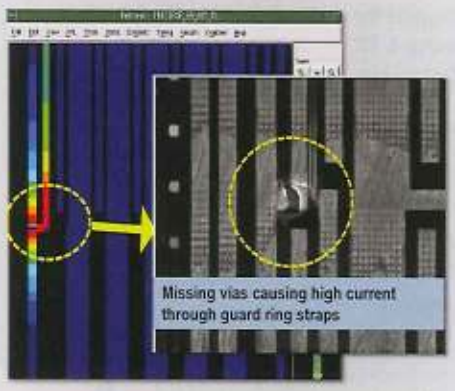
ANSYS ESD Requirements for 28nm/20nm/16nm Macro/SoC Success

Challenges

- Smaller geometries
- Higher levels of integration
- Higher pin-count
- Complex ESD protection schemes
- Multiple power islands
- Higher current density

CAPACITY	• Full-SoC capacity with package impact • Multiple PG domains
ACCURACY	• Advanced process parameter handling • ESD / snap-back device modeling
COVERAGE	• Early stage optimization to sign-off • Handle different ESD scenarios
USABILITY	• Customizable to handle design needs • Layout-based issue identification

ANSYS Interconnect Failure Analysis
Case Study

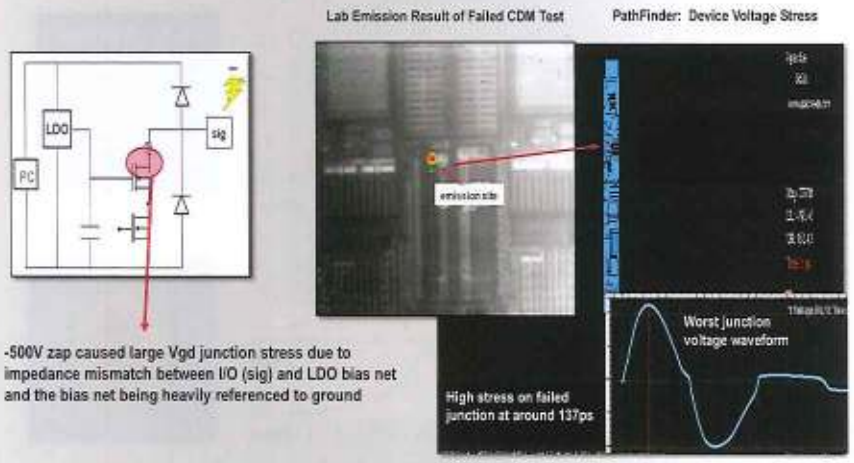




- Apache RedHawk EM-based ESD current density analysis methodology is introduced. It can provide a good results match to the real field EOS/ESD failures.
- Used as sign-off tools to verify the I/O cell ESD layout robustness for several years.

"EOS/ESD Current Density Analysis Methodology for Robust I/O ESD Network Design" - 2013 International ESD Workshop , Chanhee Jeon, et.al , Samsung Semiconductors

ANSYS Transient Simulation Based Checks



-500V zap caused large Vgd junction stress due to impedance mismatch between I/O (sig) and LDO bias net and the bias net being heavily referenced to ground

"ESD Dynamic Methodology for Diagnosis and Predictive Simulation of HBM/CDM Events"
–EOS/ESD symposium 2012, "Ting Ku, et al, Nvidia Inc.,"

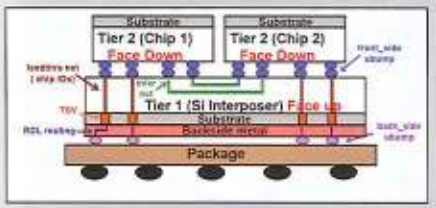
ANSYS Collaboration on ESD Verification with TSMC

- SoC static ESD Verification (since TSMC Ref flow 11.0)
- I/O level R and current density check
- SoC-level R and current density check with fast turnaround time
- Dynamic ESD check on I/O (ongoing)
- Apache supports 20nm ESD rules with TSMC provided clamp info.

ANSYS Outline

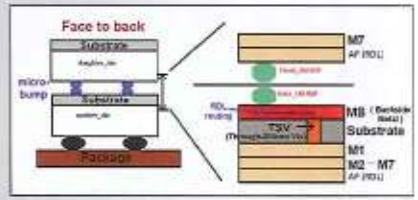
- IR/EM Support for Emerging 20nm, 16nm FinFET
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ANSYS From CoWoS to 3D-IC Designs



Silicon Interposer-based 2.5D Designs

- Standard chips on passive TSV interposer
- Mixed fab process
- Lower cost
- Will be used the most in the next decade



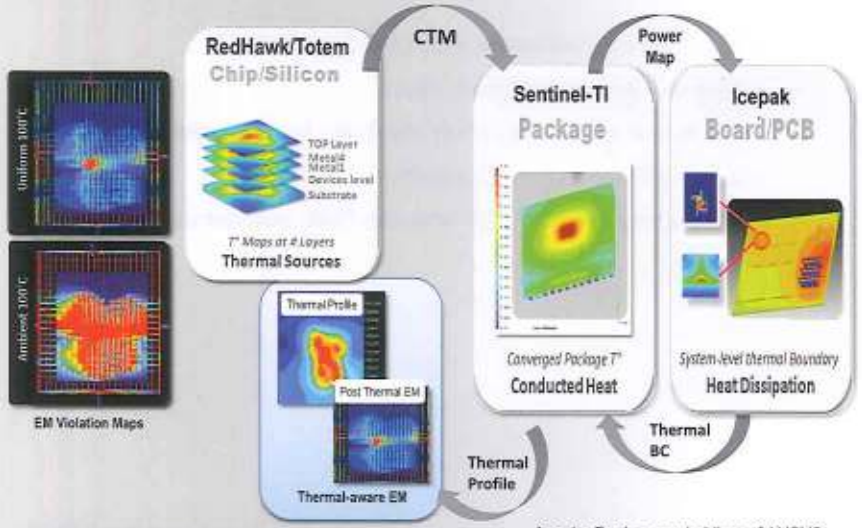
Vertically Stacked Die (3D-IC)

- Standard chips on active TSV chips
- Better performance
- More expensive (TSV chips)
- Need ecosystem, EDA, and business model

Courtesy of TSMC Reference Flow

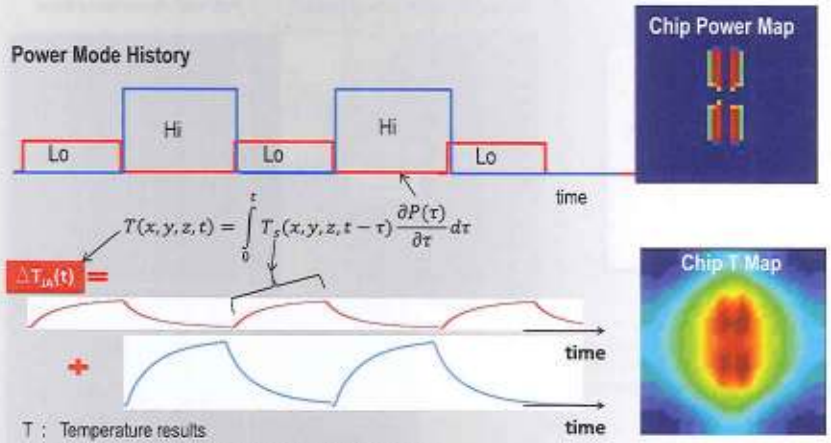
next

ANSYS 3D-IC Thermal Integrity



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ANSYS Thermal Responses Due to High/Low Power Mode Switching

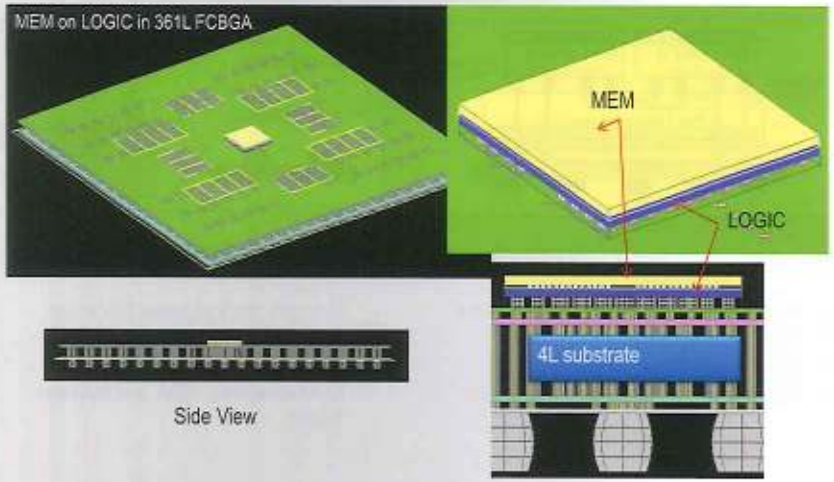


T : Temperature results
Ts: Temperature response for power on, a step change
P : Power (map) on in chips

- **Optimize thermal sensor placement**
- **Accurate Tmax determination**

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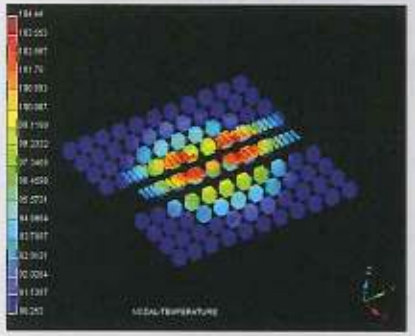
ANSYS Reference Flow 3D-IC Package Configuration



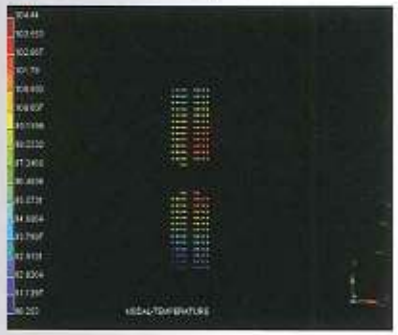
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ANSYS Temperature Map of Micro-bumps and TSV Under MEM and LOGIC Die

Micro-bumps Temp Map



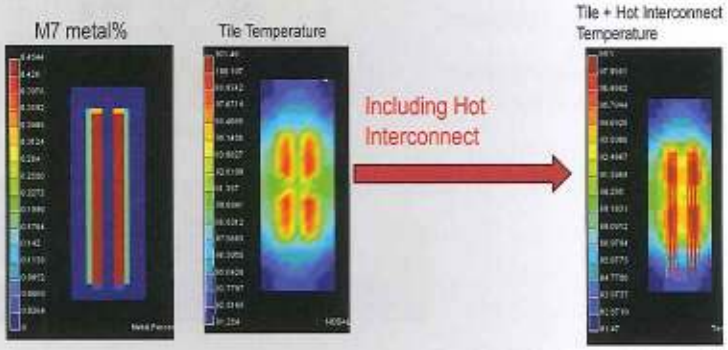
TSV Temp Map



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Hot Interconnect Temperature Profile

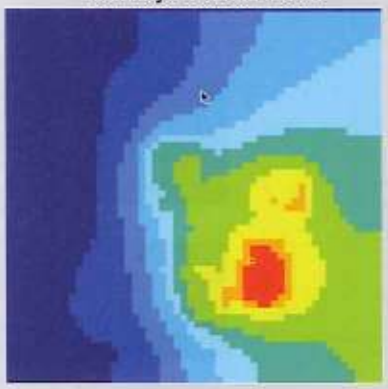
- Thermal analysis can include detailed hot interconnects with consideration for self-heating power and neighboring wire thermal response
- Accurate hot interconnect thermal profile improves thermal-aware EM analysis



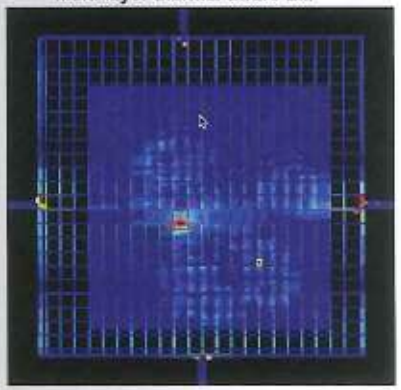
Back-annotation of Thermal Profile for Thermal-aware EM Analysis

- Multi-layer thermal profile results from SN-TI can be imported back to RedHawk/Totem for thermal-aware EM analysis

Multi-layer Thermal Profile

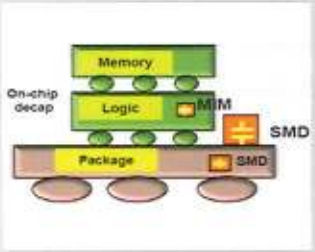


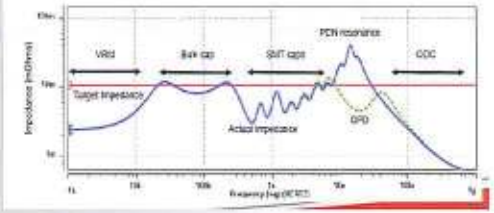
Multi-layer thermal-aware EM



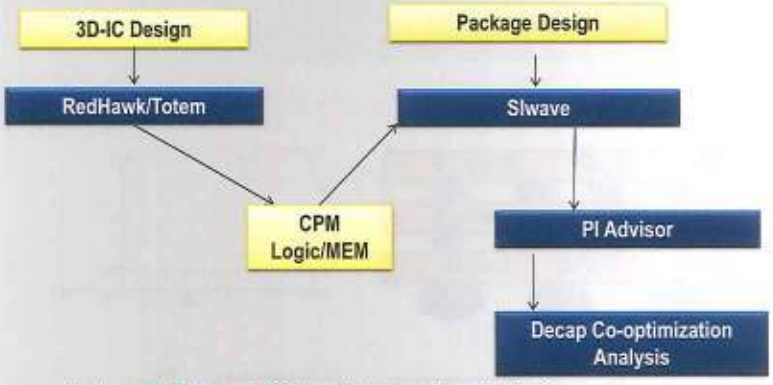
Chip-Package-System Decap Co-optimization

- 3D-IC Chip Power Model (CPM) includes both logic and memory
- Slwave with CPM import co-optimizes decap for both die and package (optionally PCB) to meet sign-off criteria with best cost-efficiency
- Performance and improvements viewed using rich GUI display





Decap Co-optimization Analysis Flow

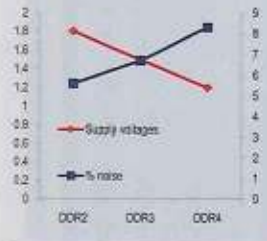


- Hook-up multiple domain CPM models and package data in Slwave
- Setup sign-off criteria on voltage drop, impedance control, or design for cost
- PI Advisor optimizes decap assignment to meet sign-off criteria with best efficiency
- Use Slwave GUI to view improved criteria performance and decap values

Impact of SSN Channel Design on Signal and Power Integrity

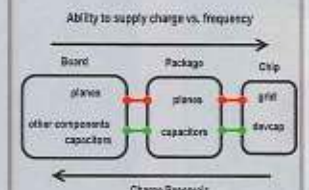
Lower Voltage

Reduces output swing
→ Lower noise margin



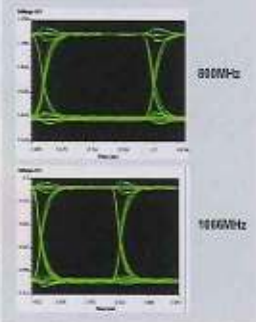
Higher Bandwidth

Requires local charge
→ Efficient on-chip decap



Higher Frequency

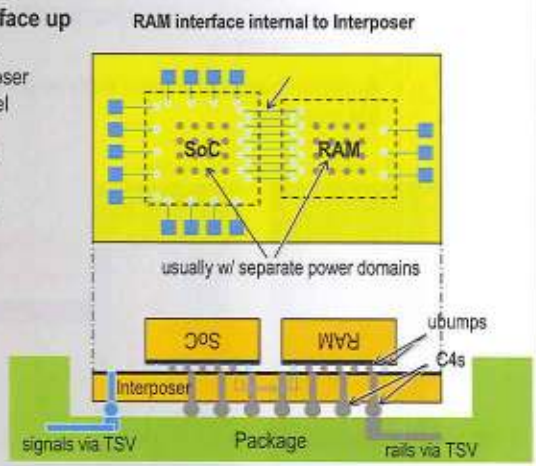
Shrinks eye size
→ Susceptible to noise



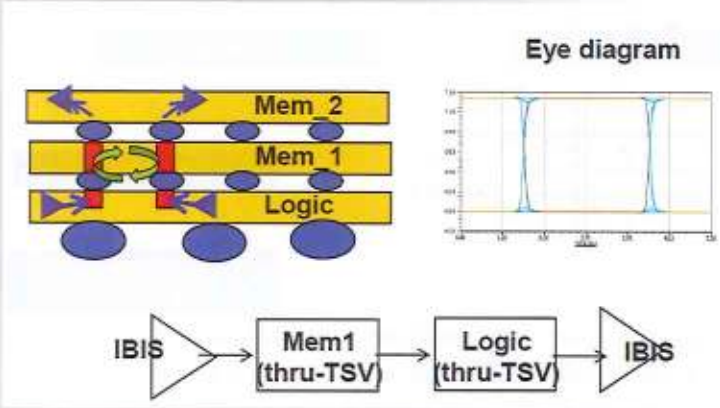
Wide-I/O on Silicon Interposer

SoC + RAM on Silicon Interposer

- **Chips face down, interposer face up**
- **Silicon Interposer connects:**
 - to chip µbumps through interposer channel for parallel bus channel (1k-8k bits)
 - chip µbumps and TSV through front-side wiring
 - to package through TSVs and C4 solder balls on back-side



TSV Stack SSN Analysis for Vertically Stacked Die



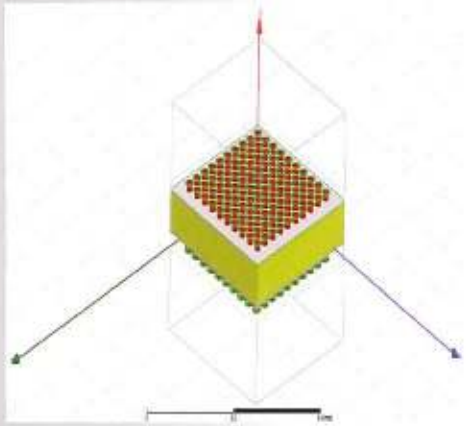
TSV Stack SSN Analysis Methodology

- **Extract vertical TSV/ubump/vias to form power/ground/signal connection path**
- **Fast extraction for large TSV array with accurate 3D EM models to capture freq dependency and crosstalk**
- **Connect TSV model, S-parameter (package/PCB), and IBIS-model for SSN analysis**
- **Analyze SI quality for vertical communication channel (> 1000s)**
- **View eye diagram and power noise in Designer GUI**

ANSYS Extract Vertical Signal Connection Path Using HFSS and/or Sentinel-PSI



One unit TSV extraction using HFSS for uniform array

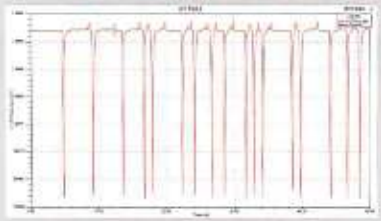


Hundreds of TSV extraction using Sentinel-PSI best for irregular spacing array

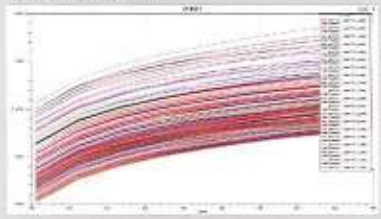
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ANSYS SSN Power Noise, Crosstalk and Eye Diagram

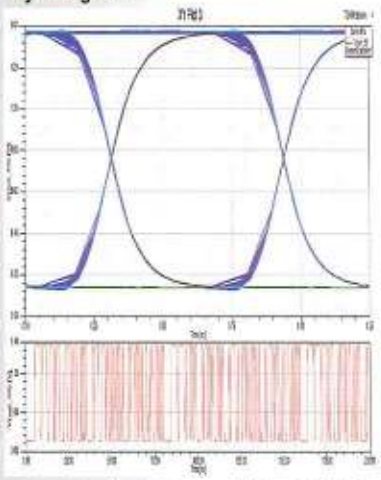
SSN Power Noise



Crosstalk Noise



Eye Diagram



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ANSYS Summary

- 20nm IR/EM support in production
- 16nm IR/EM support ready for early adopters
- Dynamic thermal analysis of 3D-IC enables thermal sensor placement, Tmax check, and thermal-aware EM analysis
- CPM import in SIwave allows global decap co-optimization for chip-package-system
- Modeling of thousands of TSV with 3D EM effect and crosstalk enables SSN analysis for vertically stacked die

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Low Power, Faster Timing ECO for Sub-20nm Designs

Dorado Design Automation

TSMC 2013
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ABSTRACT

Chip designs using 3D-IC, silicon interposer-based or vertically stacked die designs with TSVs require advanced modeling, simulation and debug capabilities to meet the demands of low-power mobile, high-performance computing, and consumer and automotive electronics. However, there are challenges in meeting these demands including verification of power, signal and reliability integrity.

With the introduction of 16nm FinFET designs, a higher current-drive and lower voltage-operation contribute to power integrity and EM reliability issues. The addition of middle layers (below M1 and above device layer) in 20nm/16nm designs can further increase the complexity in power/signal EM checking. Another concern of 20nm/16nm reliability is the need for a comprehensive layout-based full-chip ESD check to address a narrowing safe ESD design window caused by lower oxide breakdown and operating voltages. With dramatic increase in the number of on-chip supply voltages in ultra-low-power designs, the complexity of ESD protection among inter-domains is growing and needs to be automatically checked. Employing a methodology flow that provides a verification platform for 20nm/16nm designs to meet the increasing complexity of power, signal, and reliability checking is key.

From a power integrity perspective, designing the PDN to multiple die becomes more challenging with TSVs, passing power from the die closer to the package on to the die higher in the stack. The use of TSVs can cause inter-die noise and other reliability issues. This paper proposes two methods, illustrated in two different design scenarios. First, a concurrent analysis approach, where layouts of the die including the Silicon Interposer are concurrently simulated; assuming all the die data is available. The second approach is a model-based analysis, where some die data is not available, for example from an IP vendor, so a CPM is generated for co-analysis with the core die(s).

Additionally, a power related problem exists with thermal failures of 3D-ICs in a system environment. This challenge is on the operation mode switchings in mobile devices, such as on smart phones from watching a movie to reading an e-mail, the thermal signature is very different and requires a transient thermal simulation for system reliability. It is also important to decide the locations of thermal sensor placement or maximum delta of temperature between the sensor and actual location where maximum temperature occurs. A fast dynamic thermal analysis is required to help predict the actual temperature on chips in a sequence of operation modes.

From the signal integrity perspective, a significant problem has surfaced on jitter noise analysis for wide-I/O applications on Silicon Interposer and vertically stacked die designs. The requirement to have simulation of more than one thousand bits within a reasonable amount of time also demands simulation technology innovation. Apache Design has developed the CIOM as a chip I/O macro-model for fast parallel bit simulation.

In summary, a comprehensive analysis methodology is required for power, signal, and reliability issues to ensure a timely and successful design tape-out.

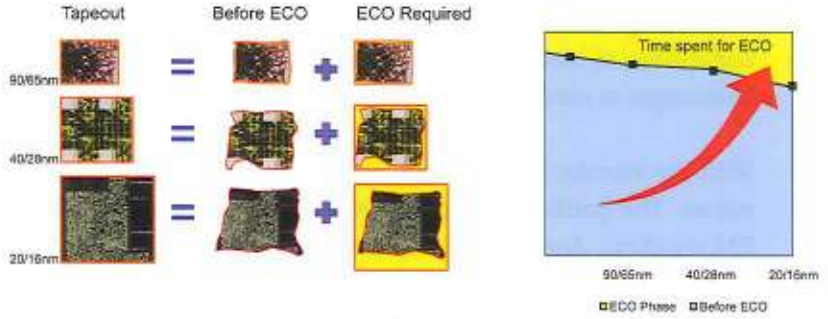


Low Power, Faster Timing ECO for Sub-20nm Designs

J.J. Hsiao, Executive VP
Dorado Design Automation, Inc.

TSMC Open Innovation Platform® Ecosystem Forum 2013

ECO Has Never Been so Significant and Important



~ Much more effort and time spent on ECO ~

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Gap to be Filled by Timing ECO at Sub-20nm



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Dorado Tweaker ECO Platform Used in TSMC Integrated Sign-off Flow (ISF)

- **Since 2010**
- **Focus on incremental optimization for "ECO Closure"**
 - **Timing ECO (setup/hold/DRV/glitch fix)**
 - **Power ECO for leakage power opt. and area recovery**
 - **Clock ECO for useful skew tuning**

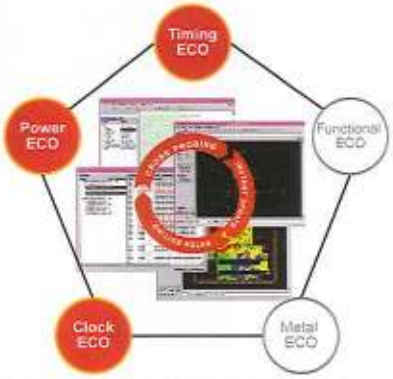


Recent Milestone of Collaboration

TSMC 20nm / Customer Tape out / 35M Instances

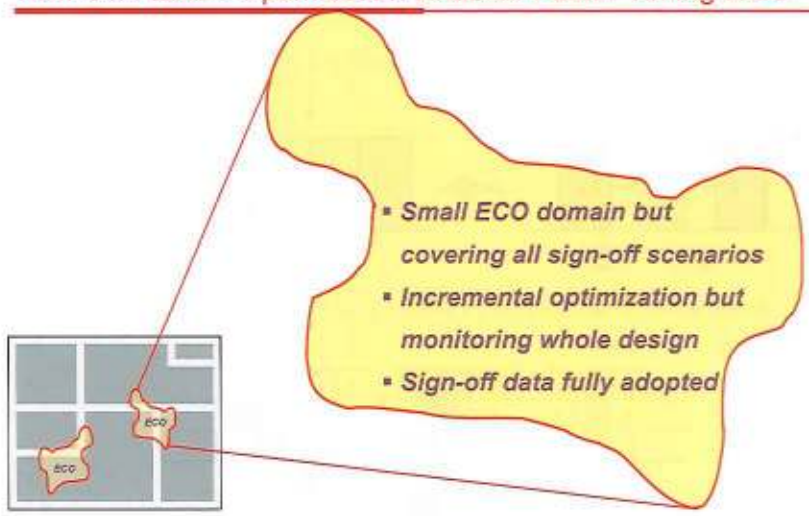
ECO strategies used in the project:

- Typical setup/hold/drv/glitch fix
- Hierarchical ECO flow for top and sub design.
- Leakage optimization + area recovery
- Manual ECO in Tweaker for special timing path
- Filler cells repair
- Post-mask Timing ECO
- Double pattering rules always honored



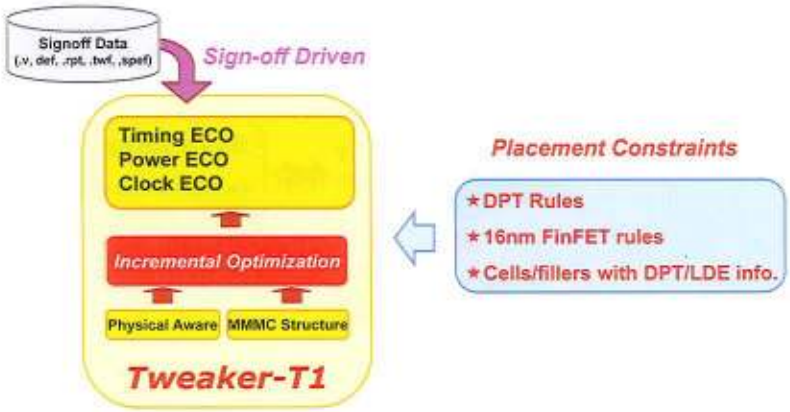
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Non-STA based Optimization Enables Faster Timing ECO



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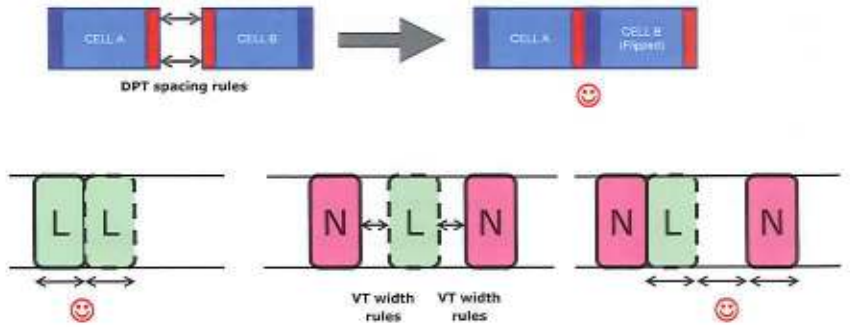
Timing ECO with 20nm & 16nm-FinFET Rules



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Basic Requirement of Sub-20nm Timing ECO

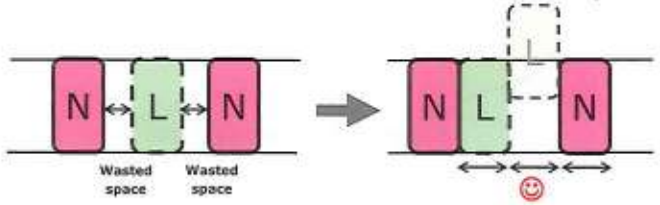
ECO with the placement constraints always honored



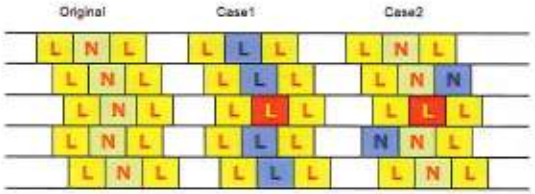
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Challenges of Sub-20nm Timing ECO

How to meet the placement constraints without wasting area ?



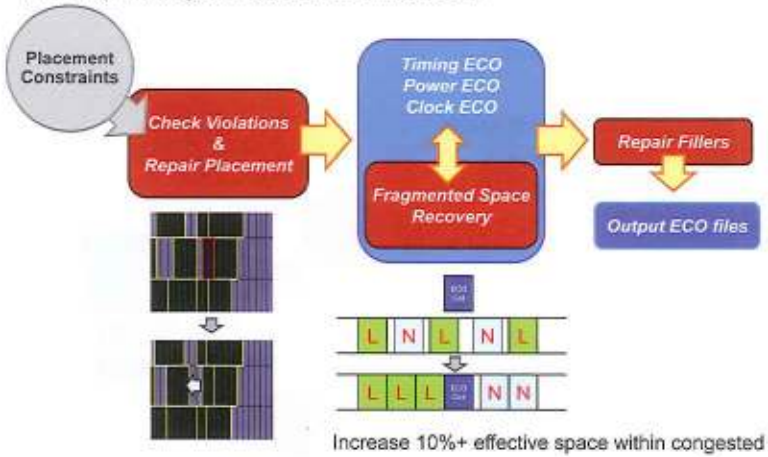
Ripple Effect caused by swapping: (or the swapping was blocked by placement constraints)



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Utilization Driven Sub-20nm Timing ECO Flow

Not only Timing but also the Utilization!



Increase 10%+ effective space within congested zone

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Features Ready for Sub-20nm Timing ECO

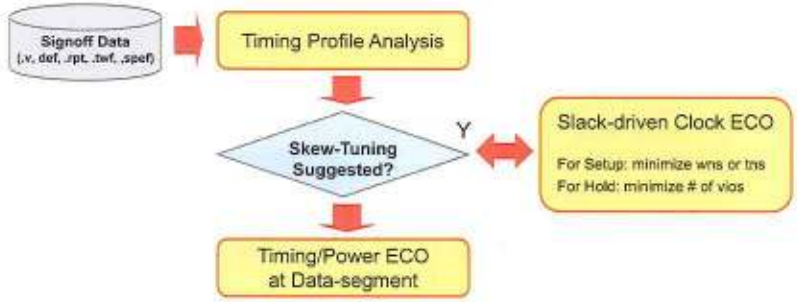
Features	Descriptions
Fix Setup	Swapping/Sizing/BypassBuf/Repeaters/SplitLoad
Fix Hold	Swapping/Sizing/DummyLoad/HFI/InsertDelay
Fix Max. Trans/Cap/Glitch	Swapping/Sizing/HFS
Leakage Opt./Area Recovery	Swapping/Sizing/RemoveBuf/RemoveInv
Skew-Tuning	Swapping/Sizing/DummyLoad/InsertBuf
Metal ECO Flow	SpareCells+GateArray
ECO Place	Place functional eco cells for timing check & fix
HackSDF	For early PostSim

All Placement Constraints transparent to users

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Extract Timing Profile to Decide the ECO Strategies

Timing ECO first? or Clock ECO first?

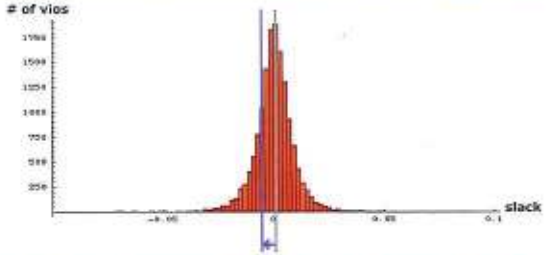


- Pre-Analyze timing vio's for fixing timing with **minimum resource**
- **Less area overhead** and more power saving with Clock ECO

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Apply Useful Skew to Minimize ECO Overhead

- For Setup: Choice of minimizing WNS or TNS
- For Hold: Minimize the number of violations under -10ps slack

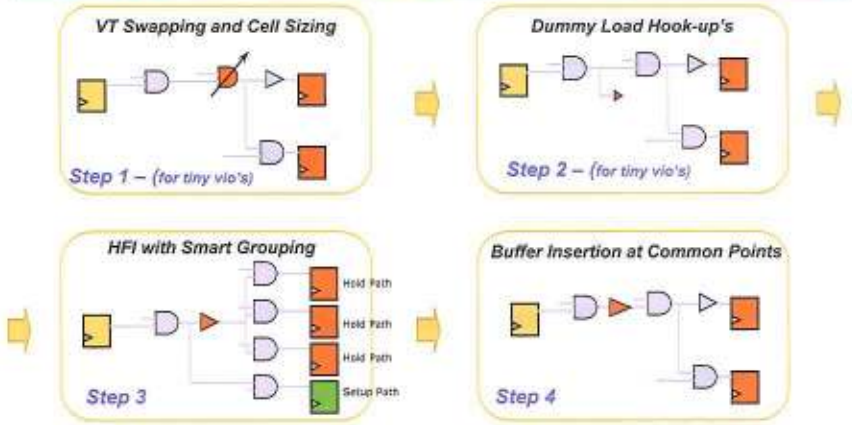


Slightly shift "zero slack" axis will remove ~15% Hold vio's with no cost of buffers

- SZ, BI, DMY Loads
- Enable automatic skew fine-tuning before setup/hold fixing on data segment

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Lower Overhead Means Lower Power



~~ Advanced hold time fixing strategies with minimum overhead!!! ~~

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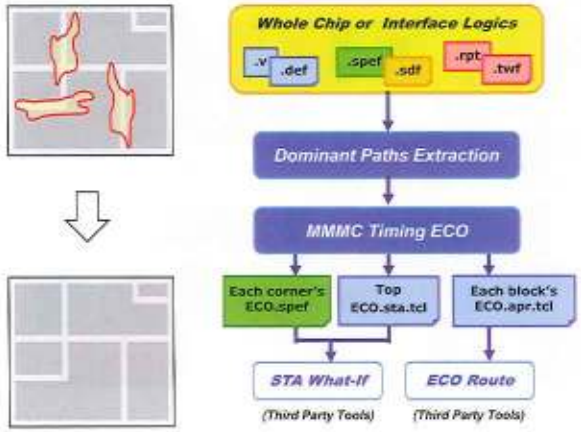
Example – TSMC 20nm / Customer Design / DMY Load Hold Fix

627K Insts	Dummy Load v.s. No Dummy Load		
Fix Hold	With dummy cells	Without dummy cells	
Vt-swap count/ Hold R2R endpoint	16 1267 -> 1253	16 1267 -> 1253	
Add dummy count/ Hold R2R endpoint Area change (um2)	1101 1253 -> 196 130.02	N/A	Slack range : -10p ~ 0 Max distance : 10um Max dummy count for each net : 2
Delay insertion/ Hold R2R endpoint Area change (um2)	1407 196->48 565.36	2513 1253 -> 48 826.96	
Total Area grow up (um2)	695.38 Save 16% area	826.96	
Run/Mem	15m/7.7G	15m/7.7G	

- Save 16% area overhead (~15 mins)
- VT width and abutment rules are both honored during Hold ECO

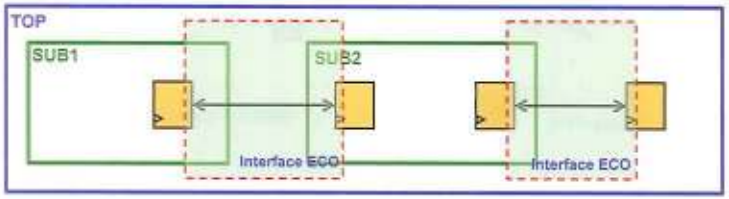
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Faster ECO Closure for Gigascale Chips



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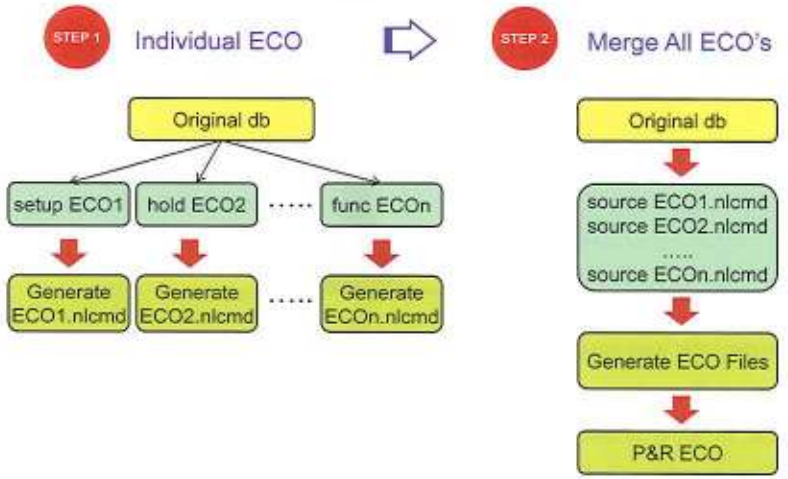
Interface Timing/Leakage Optimization



- Focus on interface logic for faster ECO closure
- No interface logic extraction needed
- No sub-design modelling required

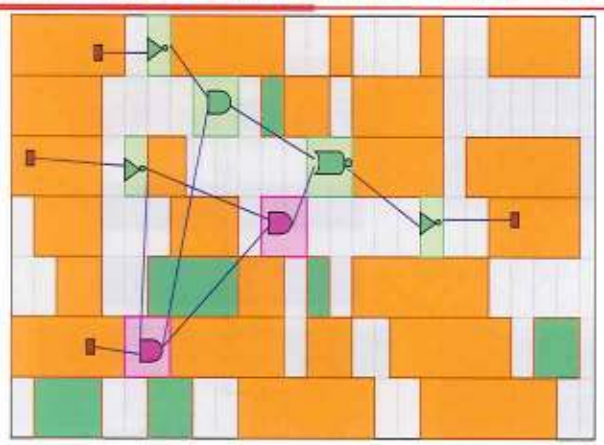
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Faster ECO Closure with Team Collaboration



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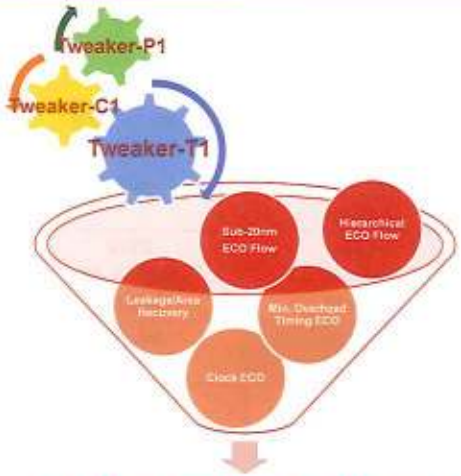
Post-Mask Timing ECO with Spare/GateArray Cells



Spare cells | Spare cells in use | Gate-array cells in use

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Summary



Low Power and Faster ECO Closure

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FinFET Modeling and Extraction for 16-nm Process

Synopsys

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ABSTRACT

FinFET technology promises to propel CMOS process scaling and modern IC design to new dimensions. FinFET's advanced 3D transistor architecture provides a unique combination of higher performance and lower leakage, but requires fundamental enhancements in process modeling and tools capabilities to realize these advantages. In this presentation, Bari Biswas will discuss the results of a multi-year collaboration between Synopsys' StarRC extraction team and TSMC to deliver a highly accurate next-generation extraction solution to accelerate development of library cells, IP and memory designs in TSMC's 16-nm FinFET process. The presentation will cover details of the StarRC FinFET solution including uniquely accurate 3D process modeling and characterization, advanced features for signoff as well as strong links with Synopsys' TCAD and spice simulation solutions.



FinFET Modeling and Extraction for 16-nm Process

TSMC OIP Ecosystem Forum

Bari Biswas
Sr. Director, R&D
1st October 2013

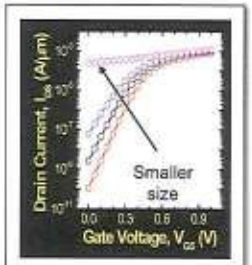
Outline

- FinFET Market Drivers
- TSMC Collaboration and Synopsys Solution
- StarRC FinFET Extraction and Modeling
- Summary

Why FinFETs?

Market Drivers

- Physical limits in scaling planar MOSFET
 - Decreasing mobility
 - Increasing gate and sub-threshold leakage
- FinFETs enable products with higher performance and lower power
- There are alternatives, but FinFET promises better Moore's Law continuation



FinFET Impact on IC Design

FinFETs' impact is largest below Metal 1

Double patterning, restricted design rules, layout dependent effect while often associated with FinFETs, are not unique to them – they are also necessary for planar technologies

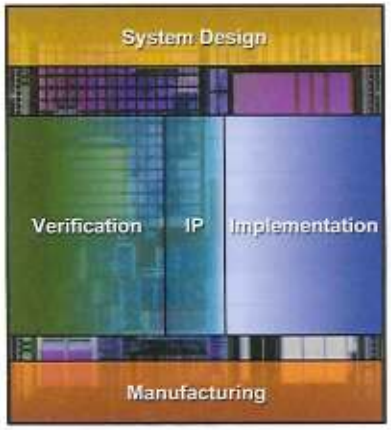
Key Areas of Impact

Foundry: Lithography, process modeling
IP design: Standard cells, memory
Custom design: Transistor-level blocks
Tools: Device and MEOL (Middle of line parasitics)

A strong collaboration with foundry is must to address new challenges and provide a complete technology, design and IP solution

Synopsys Complete FinFET Solution

Includes IP, EDA tools and manufacturing tools



Foundry-standard EDA tools

- TCAD, lithography simulation and yield management
- Extraction, SPICE, router and signoff
- Ecosystem collaboration

Extensive verification tools

- Logic simulation, SPICE, and hardware

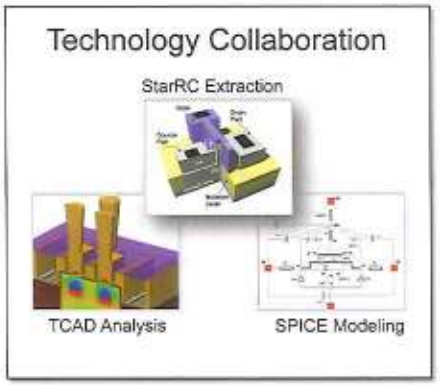
Proven IP

- Logic, memory and high speed interface

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Strong Collaboration with TSMC on Foundational Technologies





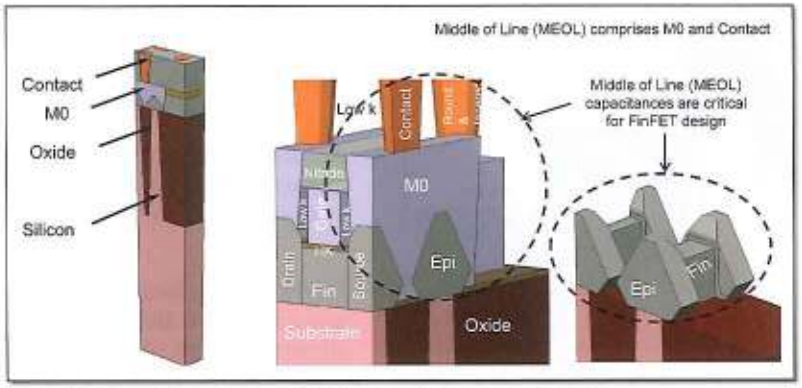
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FinFET Parasitics — A Key Challenge

3D structures introduce new capacitances that impact circuit performance

MEOL* capacitances become more complex & significant vs. planar

Capturing fin details and geometry shapes critical for accuracy



Courtesy: Synopsys TCAD Sentaurus – Enabling detailed understanding of MEOL effects

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StarRC FinFET Extraction Solution



Modeling
MEOL vs. FEOL

Layout Support
Planar vs. FinFET

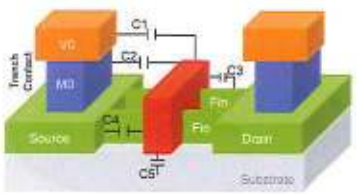
Extraction
3D, Signoff

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FinFET Parasitic Modeling

- Dedicated MEOL parasitic modeling of complex environment around device
- Coordinated modeling techniques with SPICE
 - Extract layout variant portions
 - Layout invariant portions (FEOL) using BSIM-CMG

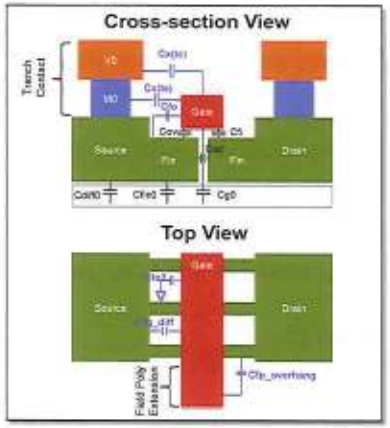
FinFET MEOL Parasitics
(Simple View)



C1, C2: Gate to contact
C3, C4: Gate to diffusion
C5: Gate to substrate

FinFET Capacitance Modeling

StarRC Extraction vs. SPICE Modeling

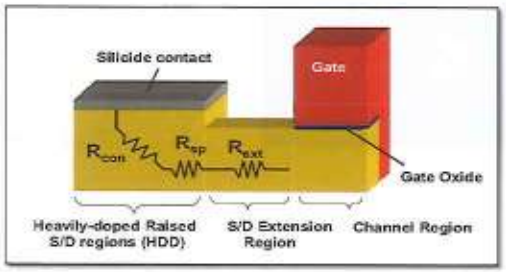


Capacitances		Tool
gate2diff	Cfo	StarRC
gate2diff	Cov, Cfi	Spice Model
diff2diff	Csd	Spice Model
gate2sub	Cg0	Spice Model
gate2sub	Cf02	StarRC
gate2diff	Cfg_diff	StarRC
diff2sub	Cfin0	Spice Model
diff2sub	Cdiff0	Spice Model
gate2diff	Cfp_overhang	StarRC
gate2cont	Cx(tc), Cx(ts)	StarRC

FinFET Resistance Modeling

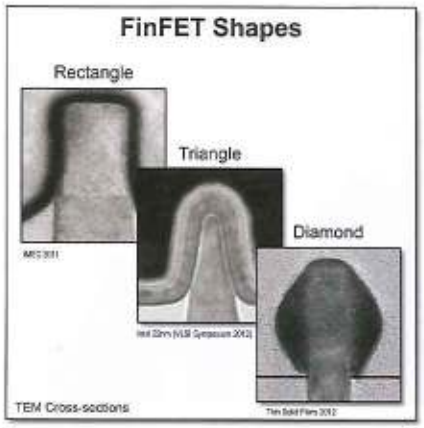
BSIM SPICE Modeling

- **Contact Resistance(R_{con}):** Combined resistance due to the raised source/drain region bulk resistivity and silicon/silicide interface resistance
- **Spreading Resistance(R_{sp}):** Resistance due to current spreading from the source/drain extension into the raised source/drain
- **Extension Resistance(R_{ext}):** Bias-dependent resistance in the thin source/drain extension region



Silicon Profile Characterization

Uniquely Accurate FinFET Modeling



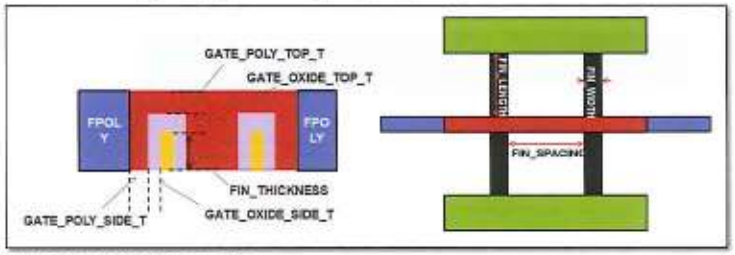
- Foundry process may support various fin shapes with distinct electrical (and mechanical) characteristics
- Accurate MEOL parasitic extraction requires detailed modeling of FinFET device
- StarRC uses silicon profile for accurate 3D modeling and characterization of FinFET

FinFET Modeling in ITF*

Ratified by Interconnect Modeling Technical Advisory Board (IMTAB)

New keyword "**MULTIGATE**" to define FinFET properties

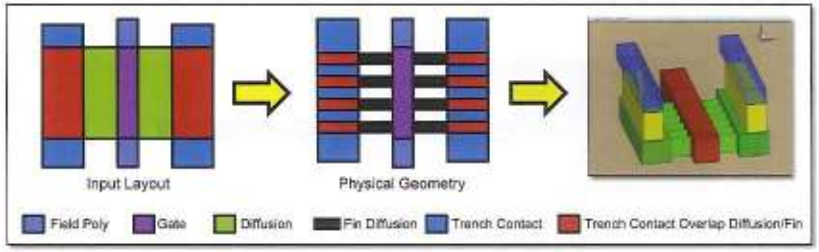
```
MULTIGATE fin1 {
FIN_SPACING=xx
FIN_WIDTH=xx
FIN_LENGTH=xx
FIN_THICKNESS=xx GATE_OXIDE_TOP_T=xx
GATE_OXIDE_SIDE_T=xx GATE_OXIDE_ER=xx
GATE_POLY_TOP_T=xx GATE_POLY_SIDE_T=xx }
```



*ITF: Interconnect Technology File

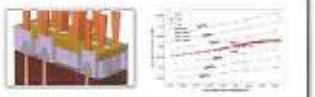
StarRC Layout Support and Extraction

- User's layout is same as planar transistor (note: quantized width)
- 3D geometry created using "FinFET profile" in ITF
- Dedicated 3D-models used for accurate extraction

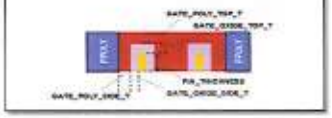


Summary: FinFET Extraction

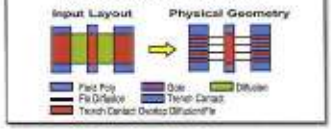
Advanced Exact 3D Modeling



ITF "MULTIGATE" Extension



Auto Layout Support

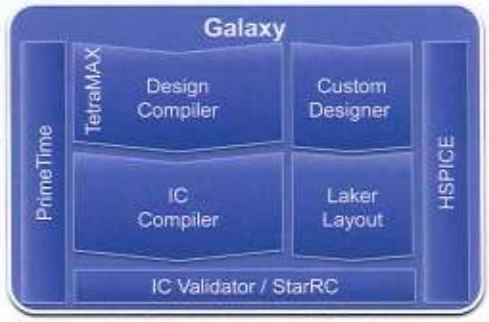


Comprehensive Solution



Tool-of-choice for major foundries!

Synopsys Galaxy Platform FinFET Solution



Function (Tools)	FinFET Readiness
Extraction (StarRC)	✓
Modeling (HSPICE)	✓
Place & Route (IC Compiler)	✓
Physical verif (IC Validator)	✓
Signoff (PrimeTime)	✓
Custom Design (CD, Laker)	✓

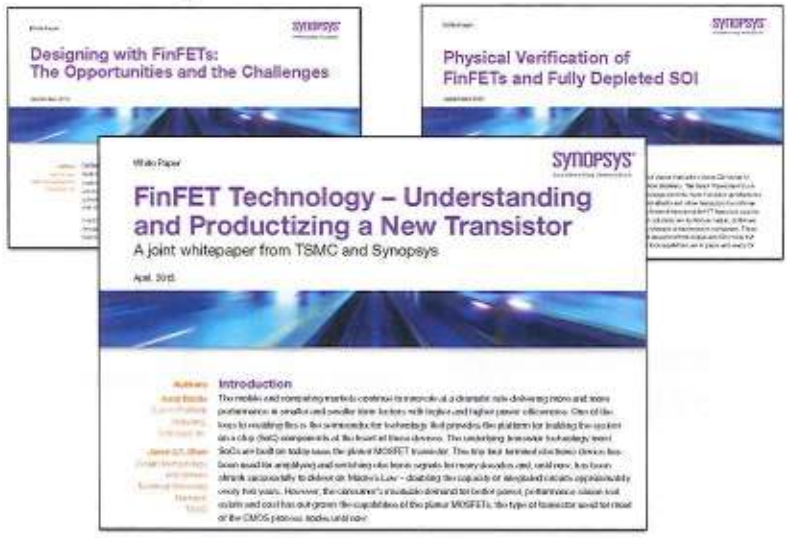
Synopsys >7 Year FinFET Experience

Industry and academia collaboration

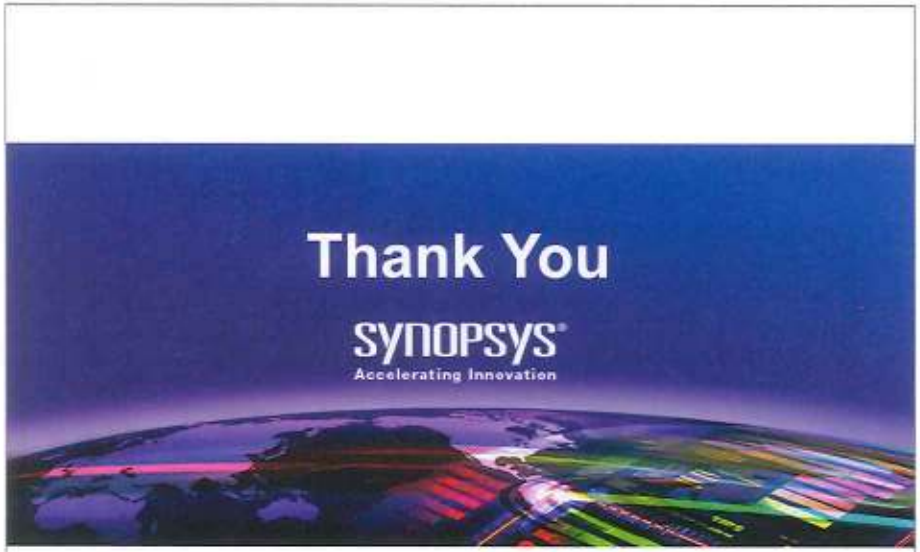


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SYNOPSYS® 25 Years

NOTE

Advanced Chip Assembly & Design Closure Flow Using Olympus-SoC

Mentor Graphics & nVIDIA

TSMC 2013
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ABSTRACT

Today, top level chip assembly and optimization is a highly iterative and manual process that can have a huge impact on design turn-around time and QoR. At advanced nodes, this problem is getting exacerbated due to the dramatic increase in the number of available transistors and increasing variability. In this session Mentor and nVidia will discuss the chip assembly and design closure solution for TSMC processes. Technology highlights include concurrent MCMM optimization, synchronous handling of replicated partitions and layer promotion of critical nets for addressing variation in resistance across layers.

Advanced Chip Assembly & Design Closure Flow using Olympus-SoC

Sudhakar Jilla
Group Director of Marketing, Mentor Graphics
Karthik Sundaram
Senior Hardware Engineer, Nvidia Corporation

Agenda

- Advanced Node Design Challenges
- Nvidia Chip Assembly Flow Challenges & requirements
- Olympus-SoC Technology & Usage
- Summary

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Design Implementation Challenges at Advanced Nodes



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Increasing Design Sizes & Functionality

- Demand for more integrated functionality & cores on a single die
- Increasing design and block sizes
- Technology scaling enables packing more transistors in the same area
- Long runtimes and scalability challenges

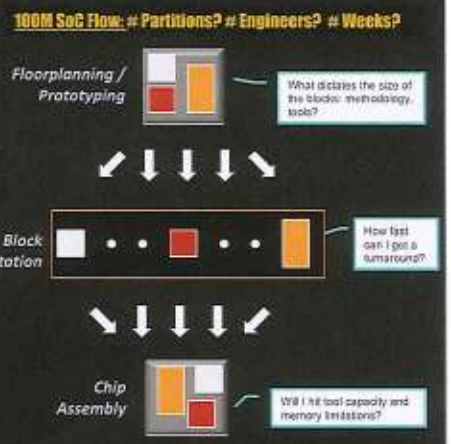


Increasing Smart Phone Functionality

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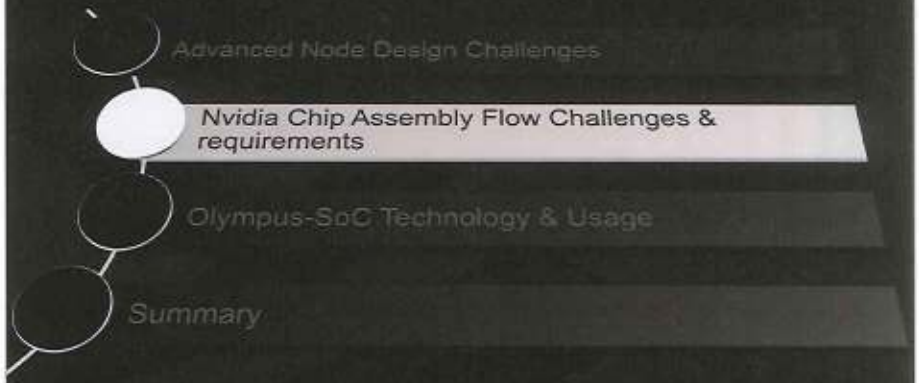
Multi-million Instance SoC Flow Challenges

- Capacity limitations to handle bigger blocks
- Long turn around time for block implementation
- Multiple iterations between block and top
- Loss in accuracy due to abstraction
- Limitations on capacity and memory for full chip



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Agenda



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Nvidia Chips

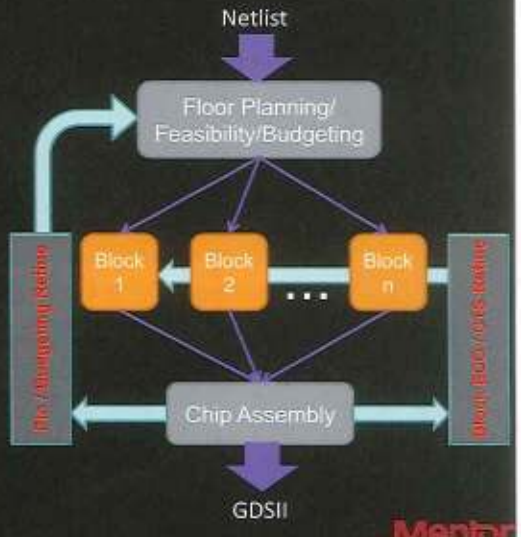


- Increasing functionality with every generation
- Reducing die area is critical for best yield
- Constant drive to increase performance
- Continuous push to lower power

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Nvidia Chip Assembly Flow Challenges

- Multiple top & block level iterations for timing convergence
- Timing closure challenges due to increasing corners/ modes/domains
- Top level CTS closure
- Memory and scalability limitations
- Timing closure TAT/runtime concern



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Nvidia Chip Assembly Flow



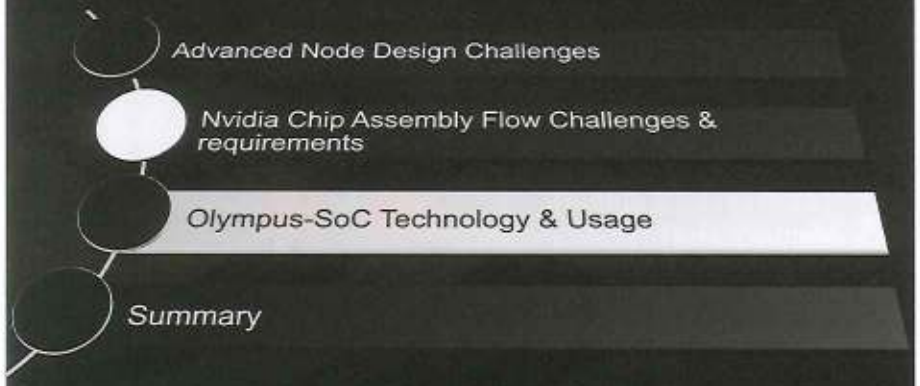
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Nvida Chip Assembly Requirements

- Flexible data abstraction
- Accurate timing budgeting
- Powerful optimization
- Efficient full chip clock tuning
- MCMM-MV aware optimization
- Memory management for big chips
- Runtime/TAT reduction by minimizing top and block iterations

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Agenda



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Key Olympus-SoC Chip Assembly Technologies

- Multiple data abstraction capabilities
- Physical aware budgeting
- Timing driven full chip clock tuning
- MCMM-MV aware chip level opt
- Timing driven port sliding opt
- Layer promotion opt for timing critical nets
- Synchronized opt for replicated partitions

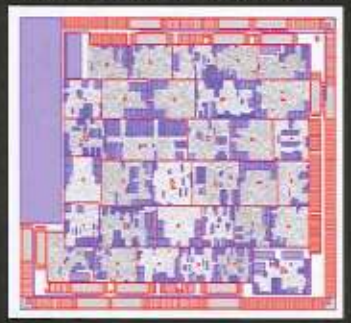
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Data Abstraction Capabilities

- Olympus supports the following abstractions:
 - Full Flat
 - Hierarchical Timing Policy
 - SI-ILM
 - Black Box Models
 - Mixed Mode

* All these abstractions help reduce memory/runtime

Full Chip Flat Timing Analysis

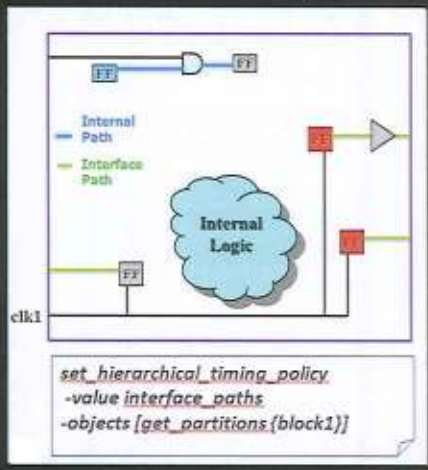


Ability to load full design and time it flat in Olympus – 143Million Gates

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Hierarchical Timing Policy (HTP)

- HTP limits optimization to the partition's interface logic
- Eliminates the need to use false paths for reg-reg paths with all partitions kept flat
- Enables efficient top level timing fixes without degrading block level timing

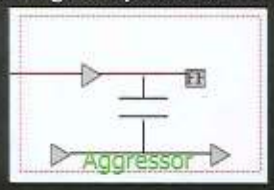



```
set_hierarchical_timing_policy
 -value interface_paths
 -objects [get_partitions {block1}]
```

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SI-ILM Generation

- SI-ILM maintains victim and aggressor nets at the interface in the model
- Observed about 25% Reduction in Memory required
- Less than 5% loss of accuracy obtained for SI timing compared to HTP

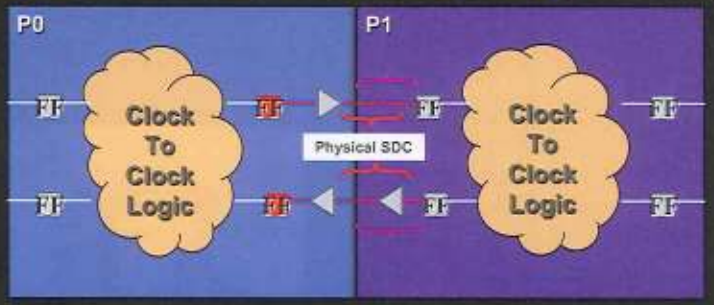


SI-ILM Flow

Generating ILM (Block Level)	• SI MODE: config_ilm -si • write_verilog –ilm • write_def –ilm • write_spef –ilm
Loading ILM (Top Level)	• read_verilog • read_def • read_spef
SI Timing Analysis & Opt (Top Level)	• Default transition for undriven nets • Infinite window for aggressor net

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Physical SDC Based Budgeting

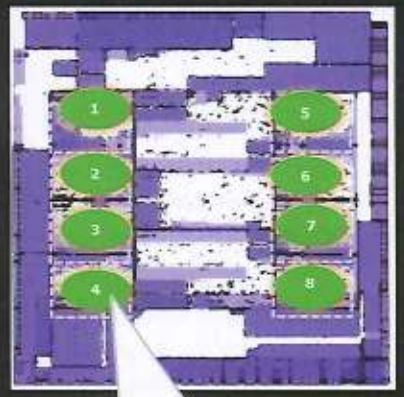


- Accurate budgeting based on Global routed and optimized interface paths
- Realistic budgets eliminates over-buffering, minimizes congestion and power
- Physical SDC Flow
 - Load full chip-pre-routed DB
 - Route all interface paths
 - Optimize for DRC & setup
 - Dump MCMM block level budgeted timing constraints
 - **Master clone aware budgeting enhancement requested

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Top Level Synchronized Optimization

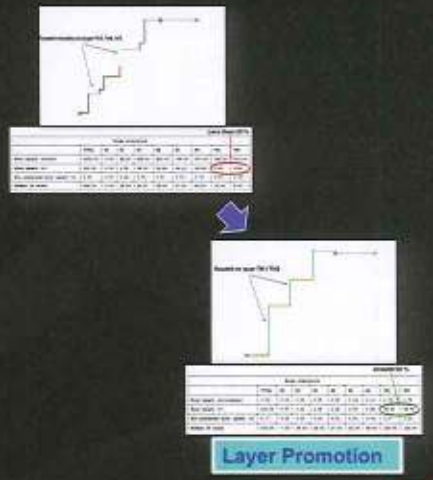
- Replicated partitions could have different requirements
- Synchronized opt - Each partition moves in "lock step" during optimization
- Maintains replication after optimization
- Fixes and validates for worst context
- Low runtime overhead for replication



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Interconnect Re-Synthesis

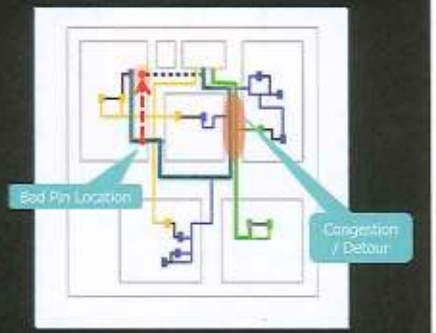
- Problem statement
 - Detours or over-buffered paths at top level
- Interconnect re-synthesis improves timing QoR at top level
 - Layer promotion for reduced resistance
 - Intelligent wire straightening & re-buffering



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Port Sliding Technology

- Timing driven block port optimization
- Reports and optimizes scenic paths by sliding ports
- Helps improve timing by optimizing port location
- Minimizes block and top level iterations
- Enhancements requested
 - Port punching support
 - Multi fan-out port sliding
 - Multi hierarchy port sliding



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Port Sliding Results

STAGE	VIOLS	SLIDABLE	WNS(ps)	TNS(ns)
BEFORE SLIDE	6961	2949	-884	-194
AFTER SLIDE	4386	374	-503	-25

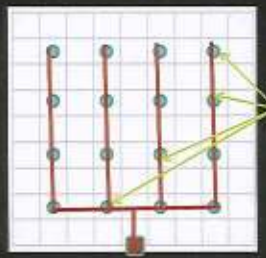
28nm GPU 15M+ Instances

- Significant improvement in timing both WNS and TNS
 - 75% WNS improvement
 - ~7x better TNS

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Top Level Clock Optimization & Tuning

- Clock latency adjustments to Partitions to improve full chip timing TNS/THS
- OCV and MCMM aware refinement
- Replication aware clock latency adjustment supported





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Top Level Clock Optimization Results

28nm GPU with 7M+Instance

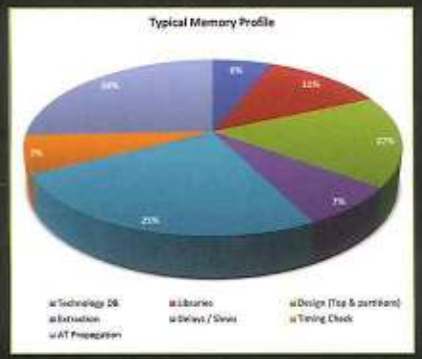
Metric	INITIAL	FINAL	CHANGE %
WNS	-1170ps	-1170ps	0
WHS	-118ps	-110ps	6.78
TNS	-212496ps	-116472ps	45.19
THS	-118582ps	-108720ps	8.32

- QOR vs Runtime tradeoffs are possible by controlling the number of Passes and Iterations

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Memory Reduction Technologies

- Delay and slew caching on disk
 - Reduced timing graph memory
- Static pruning
 - Remove slacks on paths with high margins from timing graph
- Hierarchical timing policy
 - Limits timing/ optimization to the partitions Interface
- SI-ILM



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Agenda

- *Advanced Node Design Challenges*
- *Nvidia Chip Assembly Flow Challenges & requirements*
- *Olympus-SoC Technology & Usage*
- *Summary*

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SUMMARY

- At Nvidia we use a rich feature set from Olympus-SoC for abstraction during chip assembly
- Powerful optimization recipes help reduce Iterations and improves TAT for convergence
- Olympus provides good support from CAE/R&D on their tools
- Requesting timer/optimizer speedups to enable MCMM flat optimization for faster TAT & convergence

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Mentor Graphics

Thank you!!

Questions/Comments ?

Q & A

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NOTE

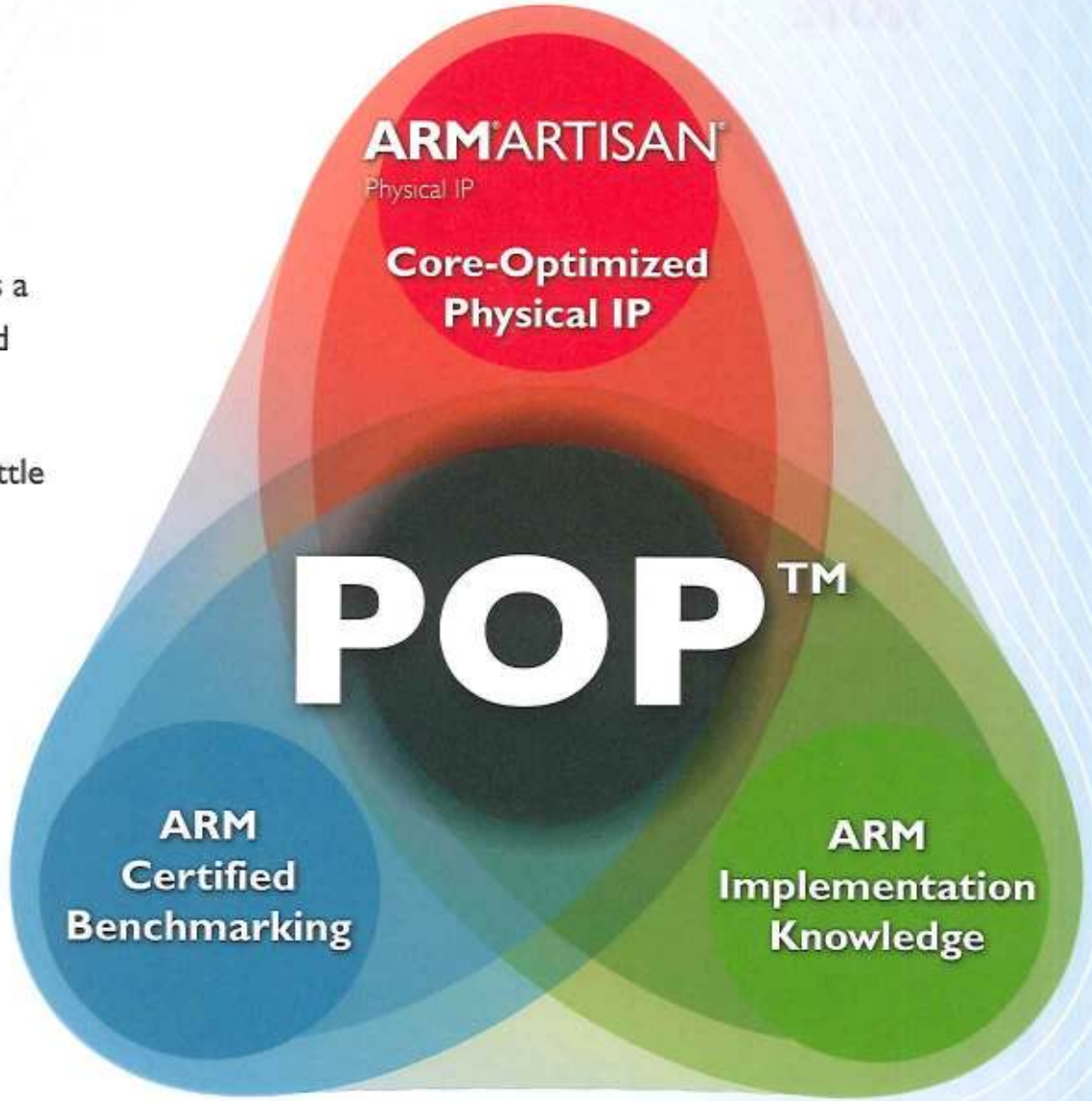
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IP Track

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Key Design Practices in IP Development of 28G SerDes Design in TSMC 28nm

Semtech / Snowbush

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ABSTRACT

The presentation will describe the methods used to devekop high performance, high quality IP as a multi-standard 28G SerDes Platform in TSMC 28nm HP/HPM. The necessary specification development, design techniques, tools and flows, and process technology are described and how this changed and adapted from 40nm to 28nm. The presentation will highlight how the process technology changes at 28nm expand the margin and offer greater performance and the how layout trade-offs are made forced by changes in design rules. Two different architectures are utilized to illustrate the best practices. A design platform targeting 12.5G on TSMC 28nm HP focusing on standards including PCIe 3.0, SAS 12G, and 10GBase-KR, and a design platform targeting 28G performance targeting standards CEI 25G-28G, FC16G, and the emerging PCIe 4.0 technology. Better ROI is illustrated by developing IP for both internal and external use and leveraging platform technology into multiple IP products and multiple chips.

SEMTECH

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Key Design Practices in IP Development of 28G SerDes Design in TSMC 28nm

Kevin Walsh – Director of World Wide Marketing Semtech-Snowbush IP
Saman Sadr – Director of Analog Design Semtech-Snowbush IP

Outline

SEMTECH SNOWBUSH IP

- **Design Objectives**
 - Process independent
 - 40nm versus 28nm
- **Design Approach**
 - Architecture
 - Design-in Quality: Taguchi Method
 - Quality Assessment: TSMC IP 9000
- **Deliverables**
 - External Customers
 - Internal Customers
- **Flows**
 - Mixed-signal
 - Signal and Power Integrity
 - Package Modeling
 - Layout & Design Checking
 - DFM and Test
- **Technology**
 - Assessment: Impact on Performance
 - Guidelines
- **Example**
 - Lessons from Practice
 - Improvements for the Future

2

SEMTECH SNOWBUSH IP

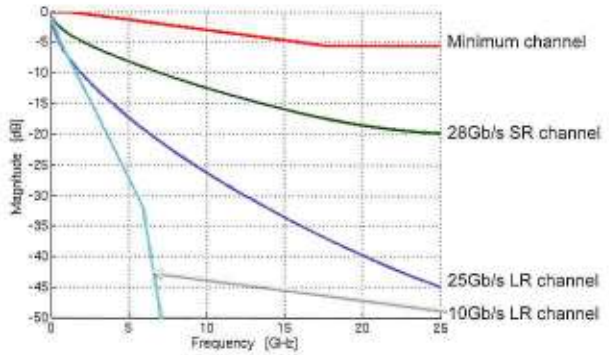
Design Objectives

3

Design Target Channels

Following Channels used During Initial System Design

SEMTECH SNOWBUSH IP



- 25Gb/s channel (OIF-25G-LR): **28dB** attenuation at **12.5GHz**
- 28Gb/s channel (OIF-28G-SR): **16dB** attenuation at **14GHz**
- Minimum channel (OIF-min): **4.4dB** attenuation at **14GHz**
- 10Gb/s channel (10G-KR): **28dB** attenuation at **5GHz**

Many 'real world' measured S-parameter channels then later stress tested

4

Transmit Jitter Specifications

SEMTECH SNOWBUSH IP

Parameter	Units	28Gbps (OIF-CEI)	25Gbps (OIF-CEI)	14.0Gbps (OIF-CEI)	11.3Gbps (OIF-CEI)	10.3Gbps (KR / XFI)
Unit Interval	ps	35.7	40	71.4	88.5	97.1
BER Target (from target standard at this rate)	-	1e-15	1e-15	1e-15	1e-15	1e-12
Golden PLL Bandwidth (OIF standards Rbaud / 1667)	MHz	16.8	15.0	8.4	6.8	4
Total Jitter	ps (UI)	11.0 (0.28)	11.2 (0.28)	21.4 (0.30)	26.5 (0.30)	27.1 (0.28)
Deterministic Jitter	ps (UI)	5.3 (0.15)	5.8 (0.15)	10.7 (0.15)	13.3 (0.15)	14.5 (0.15)
Random Jitter	ps rms (UI)	0.34	0.37	0.67	0.83	1.03
Duty Cycle Distortion	ps (UI)	1.24 (0.035)	1.36 (0.035)	2.5 (0.035)	3.1 (0.035)	3.4 (0.035)

- Actual design targeting margin above this
- For example, we are targeting a total jitter of 8.9ps (0.25UI) @ 28Gbps

40nm Versus 28nm

SEMTECH SNOWBUSH IP

- **Major Changes**
 - Layout orientation
 - Layout restrictions
 - New DFM rules
- **Design Impact**
 - Changes in electrical performance

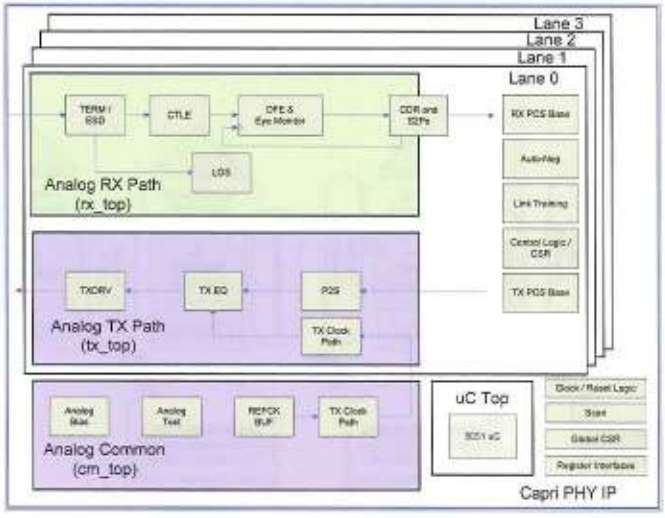
		40G	28HP	28HPM	Application
Core Vcc (V)		0.9V	0.85V	0.9V	
VT	Ultra-Low		V	V	Support high speed performance
	Low	V	V	V	
	Standard	V	V	V	
	High	V	V	V	
	Ultra-High			V	Support low leakage power for mobile applications
	Gate Length Bias	Positive only	Positive and Negative	Positive and Negative	Support flexible speed and leakage trade-off
IO	2.5V (UD 1.8V & OD 3.3V)	V	V	V	
	1.8V (UD 1.5V)	V	V	V	
SRAM	SP (HD & HC)	V	V	V	
	DP	HD & HC	HC only	HC only	

Design Approach

SEMTECH SNOWBUSH IP

Architecture – Block Diagram

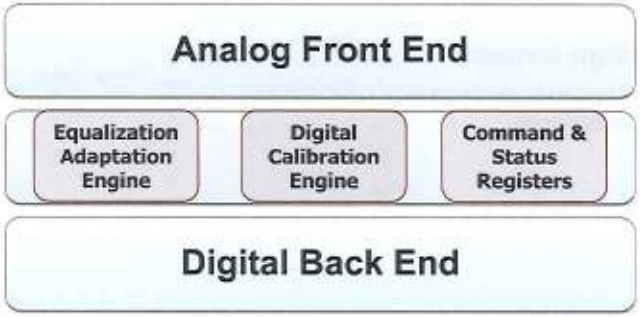
SEMTECH SNOWBUSH IP



Highly Programmable Platform

SEMTECH SNOWBUSH IP

- Analog front end and digital back end offer a high degree of programmability
- 200+ registers per lane to adjust performance and operation
- Separate functional blocks reduce implementation complexity and improve validation turn-around

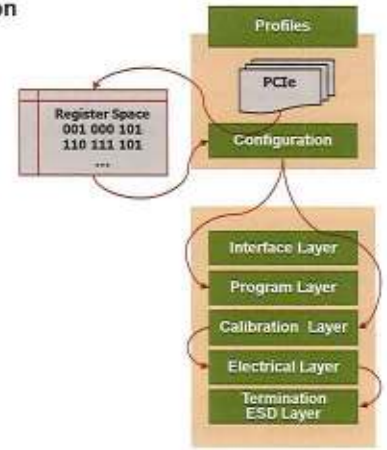


PHY Configuration "Profiles"

SEMTECH SNOWBUSH IP

- Profiles created for each supported standard reduces end-user confusion
 - Plug and play
 - Post-silicon adjustment still available
- Micro-controller provides additional flexibility to control adaptation and "soft" changes
 - Firmware provided to customers
 - Easy interface for customer processor use
- Debug and performance analysis adjustments
 - Field updates

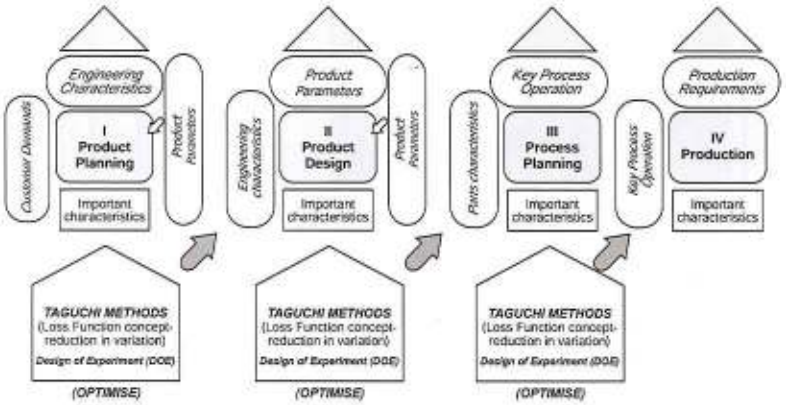
Platform Model



Design-in Quality: Taguchi Methods

SEMTECH SNOWBUSH IP

- Reduce Variability
- Manage Design Dimensions



SEMTECH SNOWBUSH IP

Deliverables

External Requirements – IP Customer

SEMTECH SNOWBUSH IP

- Design Views
- Integration Guidelines

- IBIS-AMI Models
- SPICE Package Models
- Verilog Behavioral Models

- Test Silicon/Test Chip
- Characterization and Validation
- Production Testing

Performance	Power
Area	Latency

13

Internal Requirements

SEMTECH SNOWBUSH IP

- Feature Specific Variation
- Block-level Manipulation
- Special Programmability
- Targeted Testing for Production

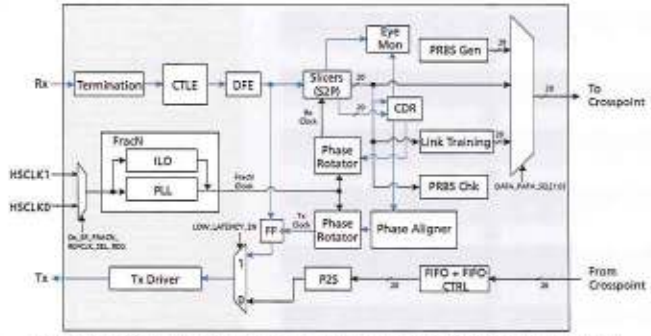


Figure A: GN2412 Family—Functional Block Diagram—Low Latency Mode (1:1 Crosspoint only)

14

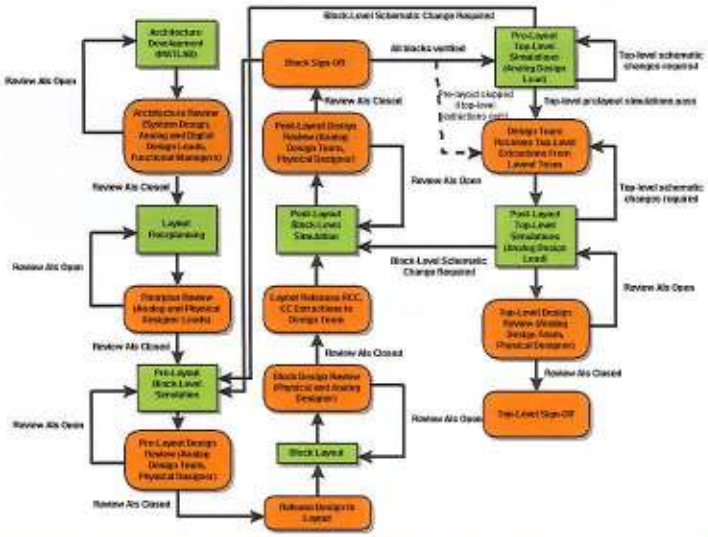
SEMTECH SNOWBUSH IP

Flows

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AFE Design and Verification Flow

SEMTECH SNOWBUSH IP



16

Design Methodology and EDA Partners

SEMTECH SNOWBUSH IP

- Initial Technology Evaluation
- Architecture & System Level Design
 - Matlab / Simulink
- Circuit Design Phase
 - Cadence / Berkeley Design Automation
- Mixed-Mode Physical Design & Verification (Layout)
 - Cadence / Tanner (Design) – Mentor (Verification)
- Digital Design & Verification
 - SNPS/ Mentor (new) & Cadence / Mentor (legacy)
- Place & Route / Extraction
 - SNPS/Mentor (new) & Cadence / Mentor (legacy)
- Reliability Analysis (Electro-migration / IR Drop / ESD)
 - Ansys Apache Totem / Cadence
- Design & Technology Correlation
- End-User System/Circuit Models (IBIS / IBIS-AMI)
 - ADS

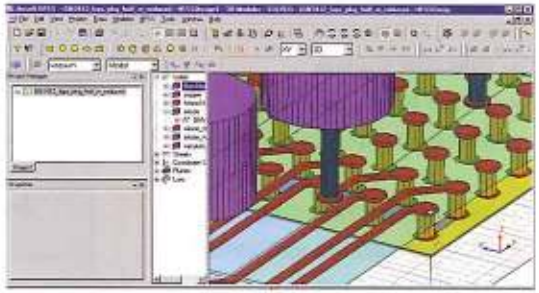
DESIGN LIBRARY	Format / Type
ANALOG	
Models	HSPICE
Verilog-A/MS Interconnect	HSPICE
DIGITAL	
Technology LEF File	LEF
Standard Cell Working Views	Verilog
Standard Cell LIB/DB Files	Lib/.DB
Standard Cell LEF Files	LEF
IO Cells Views	GDSII
VERIFICATION DECKS	**Format / Type**
Custom DRC deck	Calibre Deck
DRC waiver Settings	Calibre Deck
Custom LVS deck	Calibre Deck
Custom DFM deck	Calibre Deck
DFM Yield+ Settings	Calibre Deck
Custom Antenna deck	Calibre Deck
Custom Fill/Slot deck	Calibre Deck
Custom Floating Gate Settings	Calibre Deck
Custom Analog Extraction	Calibre Deck
RXP Layout Cell Writer	DRC Check
DESIGN TOOLS	**Tool**
ANALOG	
System Design	MATLAB
Schematic Capture	Cadence Virtuoso
Simulation	Spectre
Top-Level Simulation	UltraSim / APS
Mixed Mode/Specialty IP	Spectre
ESD Check	Spectre
Source Over/Stress Check	UltraSim / APS
Layout Editor	Cadence Virtuoso
DRC Verification	Calibre
LVS Verification	Calibre
antenna verification	Calibre
Extraction	Calibre
DIGITAL	
RTL Simulation	Questa, NCSim
Synthesis	RTL Compiler
IR Drop	ETS - Calibre
STA	RTC
Power Analysis	RTL Compiler
Equivalency Check	Conformal
DFT (Design for Test)	Encounter Test
Place & Route Layout Editor	Encounter Digital Implementation
DRC Verification	Calibre
LVS Verification	Calibre
antenna verification	Calibre
Extraction	Calibre

17

Package Modeling

SEMTECH SNOWBUSH IP

- Signal Escape
- Signal Integrity
- Parasitic Design Considerations

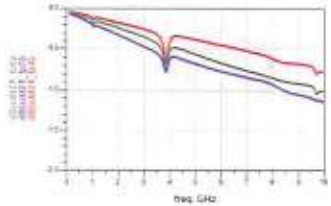


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Support for Customer Modeling

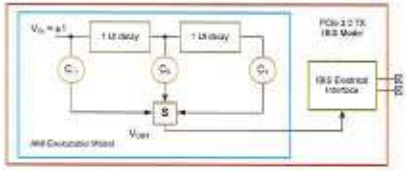
SEMTECH SNOWBUSH IP

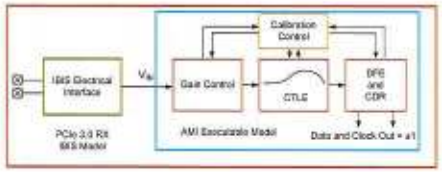
- Package Modeling: SPICE Models





- System Modeling: IBIS-AMI





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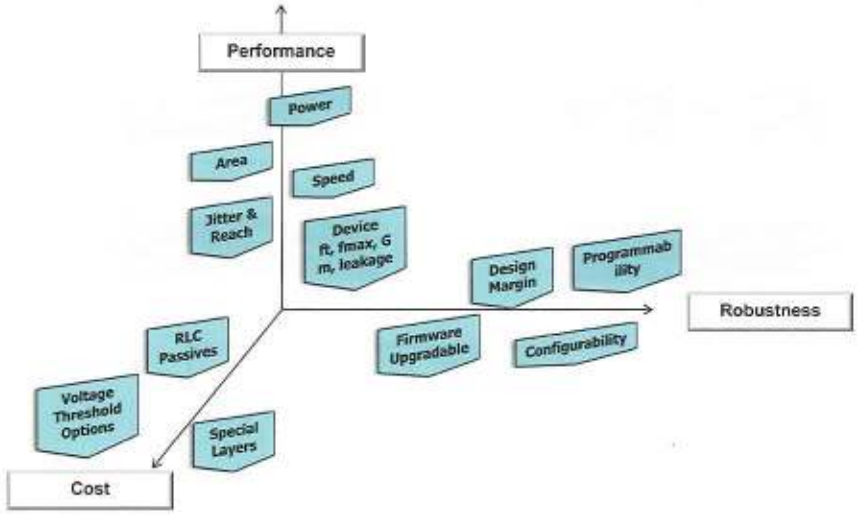
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Technology

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Key Design Dimensions

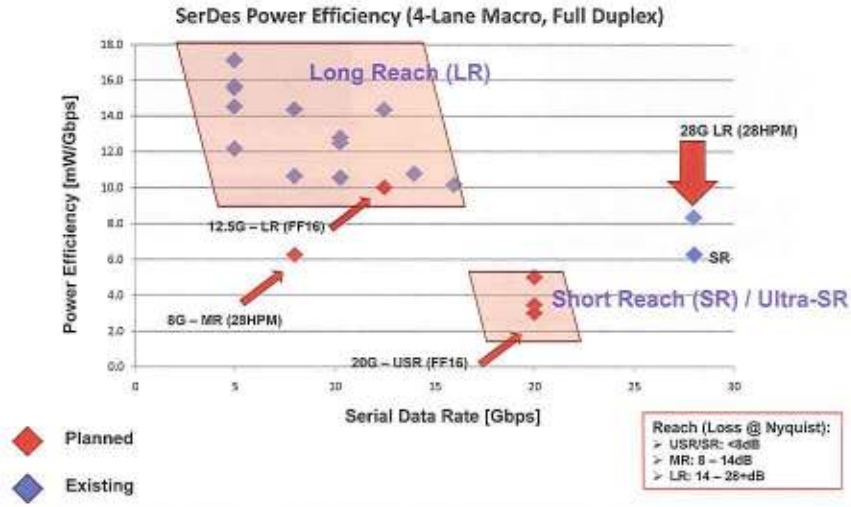
SEMTECH SNOWBUSH IP



Power Efficiency Survey

(40 LP, 40G, 28HP, 28HPM, *FF16*)

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Example – 28G SerDes

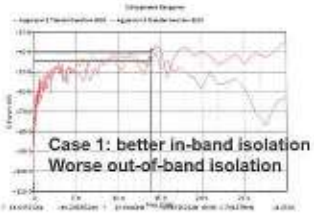
SEMTECH SNOWBUSH IP

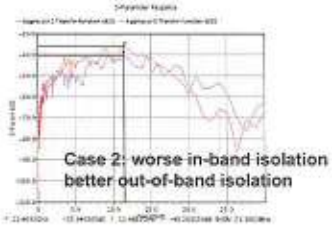
Crosstalk (1)

Example Crosstalk Response

SEMTECH SNOWBUSH IP

- Performance examined in the presence of two crosstalk aggressors (Aggressor 0 and Aggressor 1)
- Case 1: @ 14GHz
 - Aggressor 0 has **40.25dB** isolation
 - Aggressor 1 has 45dB isolation
- Case 2: @ 14GHz
 - Aggressor 0 has **35.9dB** isolation
 - Aggressor 1 has 40.2dB isolation
- Crosstalk responses for both aggressors and both cases
- Responses measured xtalk responses from real 'high performance computing' environment



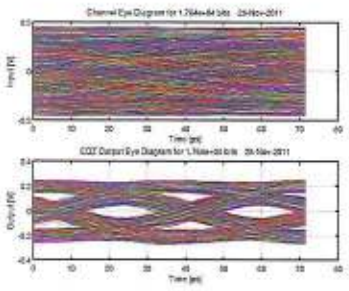


Crosstalk (2)

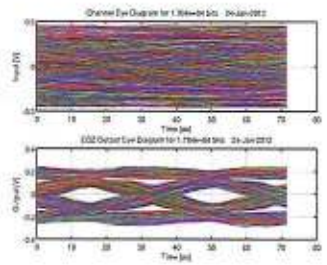
Eye Diagrams Before and After Analog Equalizer

SEMTECH SNOWBUSH IP

Case 1



Case 2



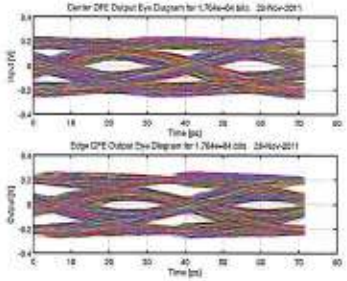
EZQ Eye	No Xtalk	With Xtalk – Case 1	With Xtalk – Case 2
Eye Height	106mV	94mV	130mV
Eye Width	0.49UI (17.6ps)	0.47UI (16.6ps)	0.40UI (14.4ps)

Crosstalk (3)

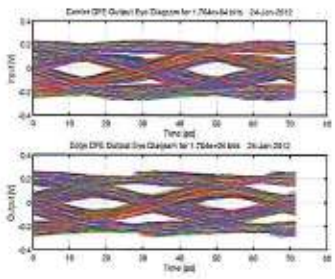
DFE Eye Diagrams

SEMTECH SNOWBUSH IP

Case 1



Case 2



Data Eye	No Xtalk	With Xtalk – Case 1	With Xtalk – Case 2
Eye Height	106mV	97mV	130mV
Eye Width	0.52UI (18.7ps)	0.47UI (16.7ps)	0.39UI (13.8ps)

Edge Eye	No Xtalk	With Xtalk – Case 1	With Xtalk – Case 2
Eye Height	76mV	61mV	97mV
Eye Width	0.49UI (17.5ps)	0.48UI (17.3ps)	0.40UI (14.4ps)

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Lessons Learned

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NOTE

16G Multi-standard SERDES IP in TSMC 16nm FinFET Process

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Ecosystem Forum

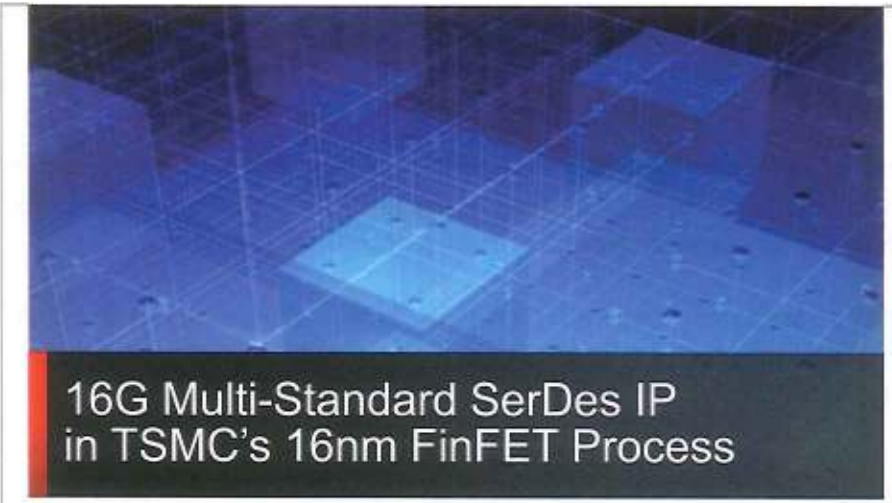


ABSTRACT

Overview of a new architecture for a high speed/PHY IP block developed in TSMC 16FF process that is running up to 16Gbps. The new architecture was designed for moderate to high loss channels (up to 30dB) for new generation of advanced processes such as TSMC 16nm FinFet.

The presentation will discuss how the acrhitecture allows a large number of decoupled digital adaption loops to take advantage of the digital performance of TSMC 16nm FinFet process. Highlights will includes how the design modifies the traditional analog / digital boundaries to reduce layout area, takes advantage of the improved gds and sub-threshold slope of the transistors while moving the requirements for critical matching to metal fingerstructures.

These Serdes/PHY design will be targeted at the next generation SoC design for high performance computing, networking,and communications systems.



16G Multi-Standard SerDes IP in TSMC's 16nm FinFET Process

TSMC Open Innovation Platform® Ecosystem Forum
Eric Naviasky, Tom Wilson, Bob Salem, Jason Chen
October 1, 2013

2013 Open Innovation Platform® ECOSYSTEM FORUM

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16G Multi-Standard SerDes

- Mainstream PCI Express Gen 4 now requires 16Gbs
- Transmission with margin through channel losses of 27dB at Nyquist is needed
- IP requires a practical and high margin solution for 16Gbs DFE, with low power, high lane count, low cost packages and boards
- Extending existing solutions runs into diminishing returns
- Optimization for FinFET nodes

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Target SerDes Design



- 1.25 to 16 Gbs data rate
- PCIe 4.0 and 10GBASE-KR Compliant
- Equalize up to 30dB channel loss
- Low power
- Highly flexible and robust
- TSMC 16nm FinFET process – 16FFLL

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Selected Challenges Surmounted in the Design

- Data and Clock Recovery in high speed, high dB loss, high crosstalk channels
- Meeting Critical loop timing for DFE
- Variability of environment and process
- Transmitter performance under low supply conditions
- High speed clock distribution

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Basic Philosophy of the Design

- Optimize block design for one function, system design for overall performance
 - Optimize paths and small blocks for speed and low power
 - Layer on accuracy through background digital calibration
 - Use simple analog blocks that don't rely on precise device characteristic knowledge (pre 1.0 PDK concerns)
- Tracking inter-stage common mode voltage for internal stages
 - Supply voltage is very low (0.715V internal)
 - No single good fixed place for common mode
- Adaption loops measure at the highest level possible and control at the lowest level possible

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16nm FinFET Design Implications (vs. 28nm)

- Much higher R_{out} (lower gds)
 - Open loop gain of stages is considerable higher
 - Common mode loops have higher gain and will require more effort to stabilize
- Device current density is a limitation. Devices are limited by metal before overdrive
- Density limitations require several iterations of layout → redesign → layout → redesign to minimize area and achieve desired performance.
- Decap is area expensive. Create less noise starting out

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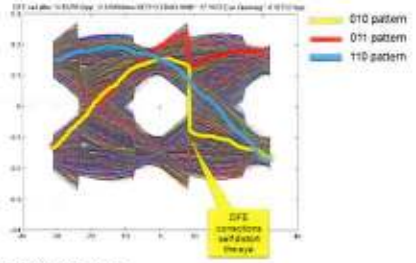
Equalization of High dB Loss Channels

- In traditional architectures, there is a limit to maximum achievable equalization
 - DFE can't begin opening the eye until clock recovery occurs
 - Clock recovery can't begin until the eye is slightly open
- Clock recovery and data recovery CTLE equalization are at odds with each other
 - High frequency peaking CTLE equalization for clock recovery amplifies crosstalk and reduces signal/noise
 - Data recovery prefers low frequency equalization to extend where the DFE can't reach
- High frequency equalization for data recovery is best provided by DFE to avoid high frequency crosstalk concentration

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Clock Data Recovery Issues in High Loss DFE Systems

- DFE corrections are nearly as large as the signal and fool the CDR
 - Corrections shift the apparent center of the eye for clock recovery
 - Obscure the real data transitions and create a blind spot
 - Narcissism will eventually will cause runaway CDR



- Equalization for data is not correct for clock recovery
 - DFE corrections are converged for data samples
 - Since DFE is a discreet time equalization, the correction value at edge samples is fundamentally wrong
- Clock recover requires high frequency equalization but is only minimally impacted by crosstalk amplification

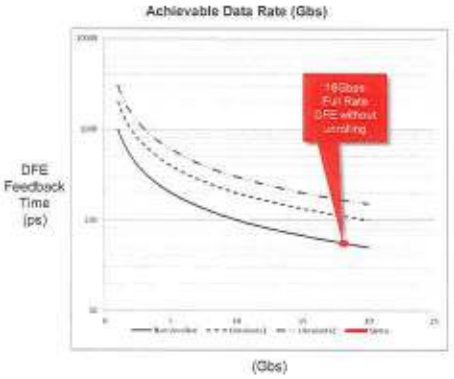
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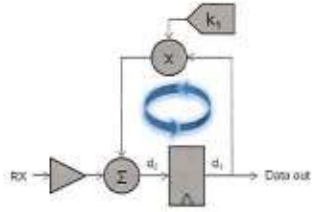
Cadence Clock Data Recovery

- Removes the limitation that the eye must be opened before recovery can begin; extends the theoretical limit of equalization
- Data recovery can be optimized for accuracy in the presence of crosstalk, clock recovery takes advantage of its inherent crosstalk insensitivity
- DFE corrections no longer obscure clock recovery loop
 - Clock recovery EQ is adapted at clock sample times
 - No blind patterns or dead spots, all edges contribute information
- Offers an additional degree of freedom; adaptive loop sets optimal data sampling point

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Data Rate



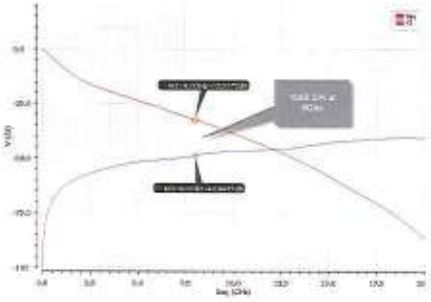


- DFE Feedback time is the time for a decision to be made and the resulting correction added to the input before the next decision can be made

- Shorter DFE feedback means higher data rate can be achieved
- Saves the power and area of unrolling circuitry

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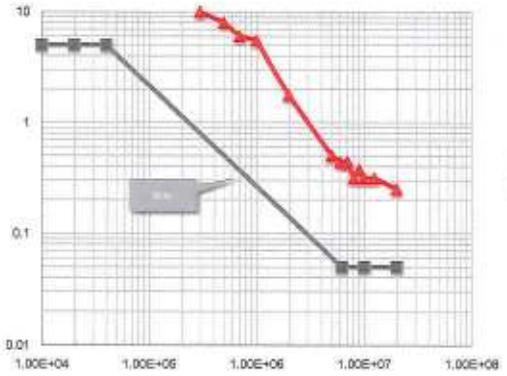
Equalizating High dB Loss Channels



- Able to equalize -32dB channels in the presence of -48dB crosstalk

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Receive Jitter Tolerance



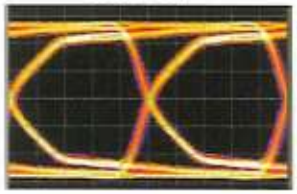
Decoupled clock recovery leads to superior jitter tolerance

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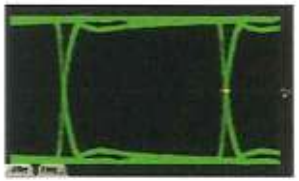
Conventional Transmitter Issues

- Transmit drive amplitude (Vppd) of H-bridge is theoretically limited to the supply voltage
- Regulators are unattractive due to power scaling and area
- Can't reduce H-Bridge power
 - Resistor divider of 200 ohms across the supply. V2/R.
 - De-emphasis *increases* the power of a voltage mode driver
 - Termination calibration, amplitude and emphasis require many resistor segments. Each has driver, cap, area.
 - CMOS pre-driver blocks are power hogs
- Need more margin
 - High freq. effects steal amplitude at transition bits
 - Real world boards have many imperfections and high loss due to economic concerns
 - Reflections, stubs and discontinuities in package/board
 - Higher loss than expected in traces up to test point
 - Stray capacitance
- Need extra margin on transmit to compensate

Output cap



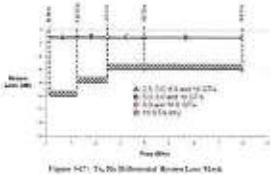
Reflections

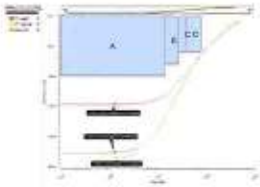


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Hybrid TX Path Solution

- Maintains power advantages inherent to non-emphasized voltage mode
- Allows additional amplitude (real emphasis) in excess of what voltage mode can produce
- Requires less power in emphasis than a conventional voltage mode or current mode driver
- Addition of broadband matching allows the use of larger and better protecting ESD diodes





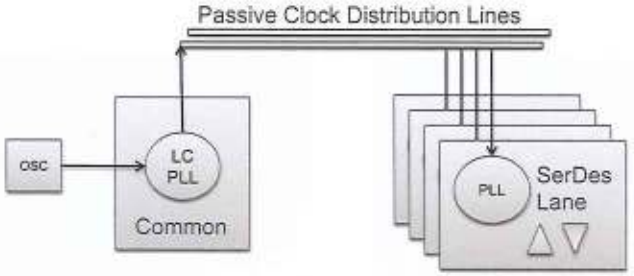
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SerDes Clock Generation Issues

- LC tank PLL is needed to achieve lowest jitter performance
- LC tank PLLs have a very narrow tuning range
- LC tank PLLs have a large area
- Applications want to provide low reference frequencies (~25MHz) to reduce cost which require LC tank performance
- Ring oscillator PLLs have a wide range, smaller area and power but can't achieve the required jitter performance without a high reference frequency
- Applications often require simultaneous multi-rate lanes within the macro, forcing a second, large LC tank PLL and clock distribution network
- Clock must be distributed over long distances from common to lanes with minimal jitter, skew, and duty cycle distortion.

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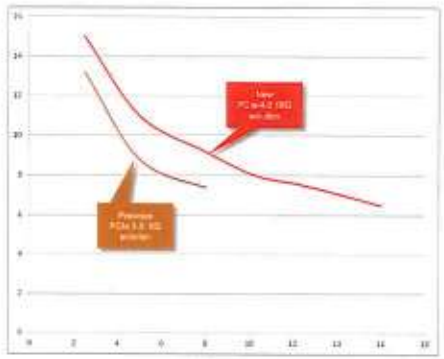
Clock generation and distribution



- Low jitter clean up PLL in common area allows the use of a less expensive reference
- Lane local digital PLL for flexible multi-rate operation, improved DCD
- Unbuffered clock distribution on high level metal avoids power supply noise induced jitter

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Power per Gigabit/Second



- Optimized for high frequency performance
- Still competitive at low data rates

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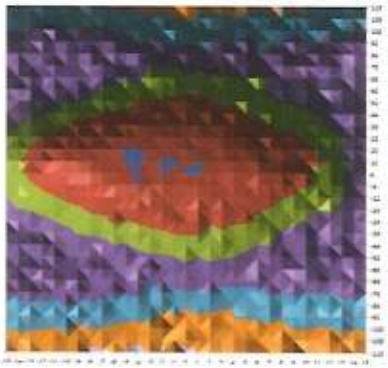
PCIe PHY IP Features
Extensive BIST and DFT

- On-Chip Oscilloscope
 - System debug with on-chip oscilloscope
 - Horizontal and vertical eye margining
- Multiple Loop Back Options
 - Pattern verifier and generator with Error Counter
 - Total of 6 At-Speed loop backs:
 - Serial, parallel, near-end and far-end and Pad Loop Back (with ISI)
- Stand-alone functionality with SoC isolation
 - PHY operational via JTAG interface
- GUI for Debug and Bring-Up
- Scan Support
 - At Speed, Stuck-at and Boundary scan capability
 - AC and DC JTAG
- JTAG, AMBA and ATB
 - On chip ADC to digitize ATB

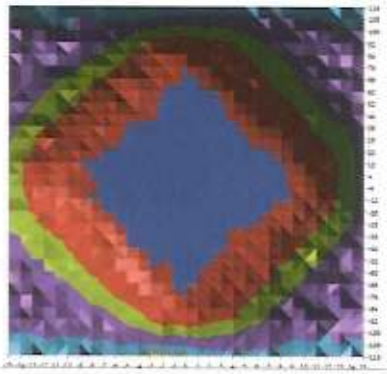
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Internal Eye Plot Capability (Eye Surf)

Before DFE Training



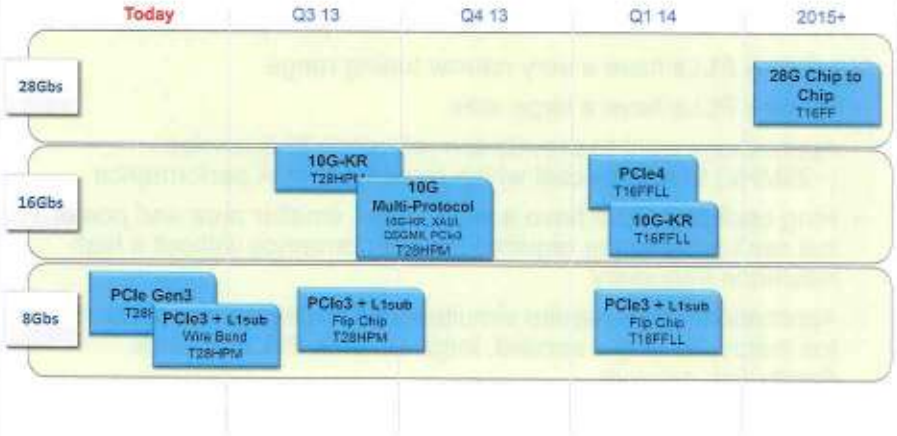
After DFE Training



- Supports on-the-fly eye and bathtub curve diagrams with 1/64UI resolution with 8-bit voltage resolution

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TSMC 16FF Enabling Higher Speed SerDes
Cadence Delivering 8 - 28Gbs SerDes



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Conclusion

- TSMC 16FF enables higher speed SerDes design
 - From 8Gbs to 28Gbs
 - Addresses emerging standards such as PCI Express Gen 4
- Cadence is committing resources for TSMC 16FF IP development across the board
- TSMC and Cadence are working together to enable the 16FF Ecosystem
- Thank you for your attention

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Hybrid Embedded NVM Solution for Flexible Product Design and Application

eMemory

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ABSTRACT

eMemory, as a pioneer in the eNVM IP segment with 180+ patents granted and more than 3,000,000 wafers shipped in TSMC, has built a sterling reputation by offering total solutions with its proprietary OTP (NeoBit and NeoFuse), Pseudo-MTP(PMTP), MTP (NeoMTP), EEPROM (NeoEE) and emb-Flash (NeoFlash) technologies. With the support of TSMC's "More-than-Moore" technologies, eMemory can offer customers maximal design flexibility and the greatest range of choices in process platforms, enabling product differentiation and giving customers a competitive advantage in the rapidly changing industry. Drawing on eMemory's extensive experience and robust design capabilities in technology and IPs, TSMC 9000-warranteed IP deliverables can be deployed for commercial, industrial, and automotive applications. With its supreme quality and excellent customer services, eMemory received 2012 TSMC Best IP Partner Award which is for the third year in a row. It acknowledges eMemory's technical capability, long-term involvement in customer projects and the commitment to quality.

NeoBit is a programmable logic device offering the industry's most proven path to embedded OTP and PMTP functionality. Key functions of NeoBit IPs widely used for chip designs are to record chip ID of IC products, or encryption key for e-payment or set-top box, or anti-piracy codes for digital right contents. Designers also use NeoBit IPs to adjust data for analog design trimming or parameter setting for product functions or boot code and firmware for microcontrollers. Key benefits of using NeoBit IPs are security, field update flexibility, product customizations, and low cost. The usages of NeoBit IPs can be found in power management ICs, Full-HD and HD720 LCD driver ICs, audio CODE ICs, and MEMS in smart phones. For applications which need seldom or frequent data update, such as function selection, parameter setting or system calibration, multiple-time write function is required. NeoMTP performs like NeoBit with electrical erase function and serves well for this rewritable purpose. NeoMTP is derived from NeoBit and can be soon ready in all NeoBit process nodes. The key feature of NeoMTP is suitable for Touch-panel controller (TPC), NB CAM controller, ASSP MCU, and fuel-gauge IC.

Most of product designs may include both one-time data setting and rewritable functions. With the demands for product design with multi-storage functions, eMemory invents a new hybride IP archtecture (NeoBit+NeoMTP), combining with high density OTP storage of NeoBit and rewritable ability of NeoMTP, to simplify the NVM IP usage for product designs with single-poly logic process.

This presentation is organized into several sections. In the 1st section, it describes eMemory's eNVM capability and availability in a broad range of TSMC process nodes to fulfill customer requirements for blooming product applications. The 2nd section introduces eMemory's core technologies, target markets and key features. The new hybride IP archtecture and advantages for product design is included in the 3rd section. eMemory's infrastructure of technical support to TSMC and its customers, technology porting to a variety of processes, and customized design capabilities are outlined in the last section.

eMemory

Hybrid Embedded NVM Solution for Flexible Product Design and Application

Evans Yang
Senior Director, eMemory
Oct. 1st, 2013

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eMemory, NeoBit, NeoFlash, NeoEE, NeoFuse and NeoMTP are all trademarks and/or service marks of eMemory in Taiwan and/or in other countries.

Outline

- About eMemory
- Comprehensive eNVM Solutions in TSMC OIP
- Core Technology and Target Markets
- Hybrid Solutions for Flexible Design & Application
- Customer Benefits, Technical Support and Service
- Summary

Corporate Overview

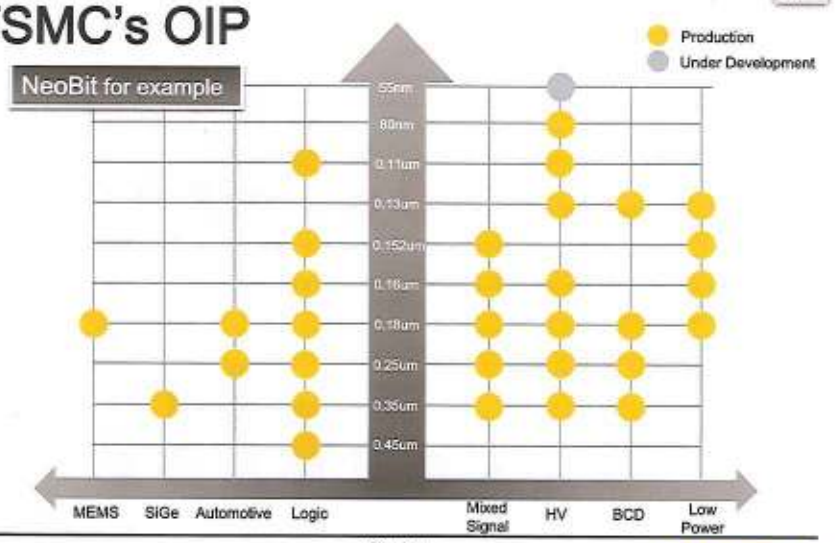
- eMemory is a Logic NVM IP provider with complete OTP, PMTP, EEPROM, MTP and Flash solutions
- 154+ NVM IP developers out of 210+ employees*
- Completed patent portfolio: 197+ patents issued, 135+ pending
- Number of IP verified: 645+
- Number of New Tape out: 2080+
- Productions: 6,000,000+ wafers shipped through Q2 '13

* As of July 2013

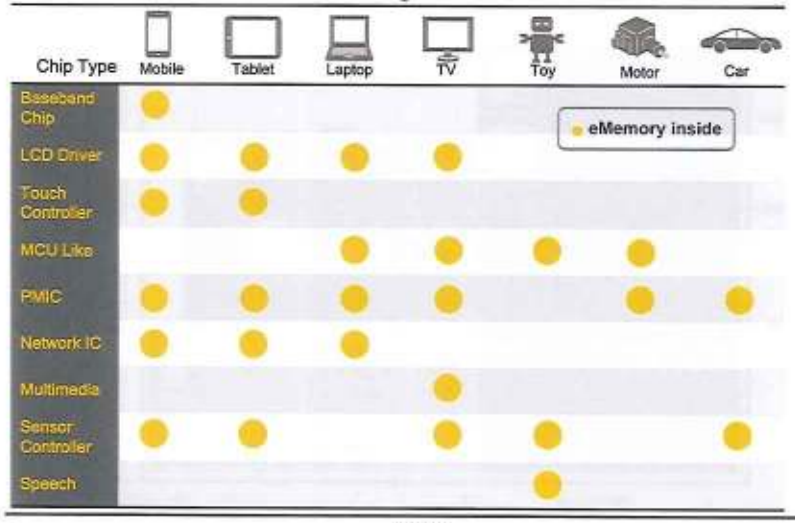
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Comprehensive NVM Solutions on TSMC's OIP



Embedded Everywhere



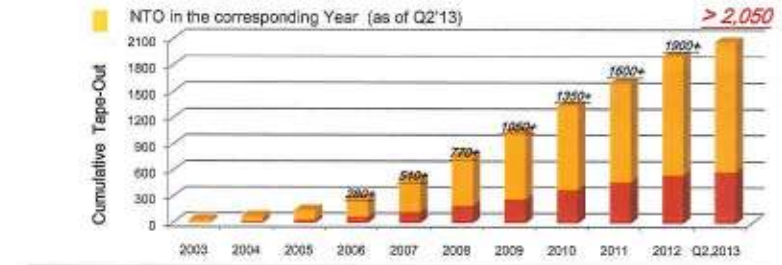
Worldwide Customer NTO 's

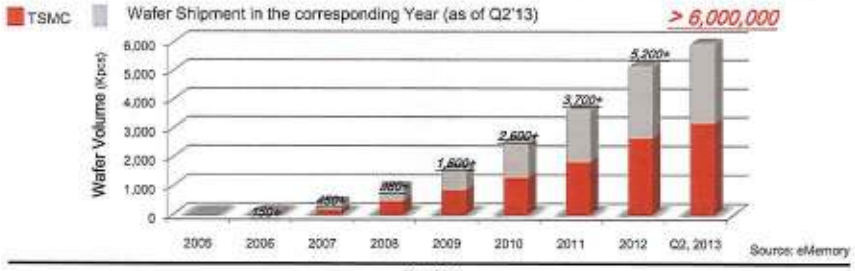


New Tape-outs (2010Q1~2013Q2)	Taiwan	China	Korea	Japan	North America	Europe	Others
Fabless NTO by Region	473	193	50	34	158	101	11

Source as of July, 2013

Wide Utilization

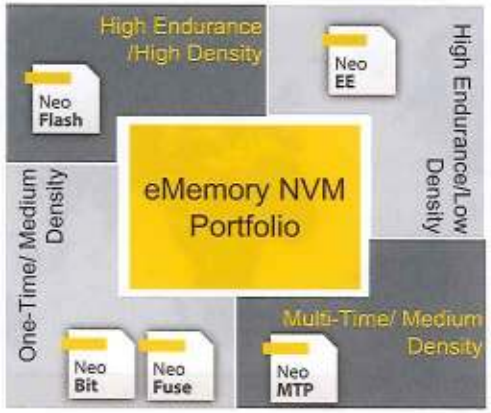




Outline

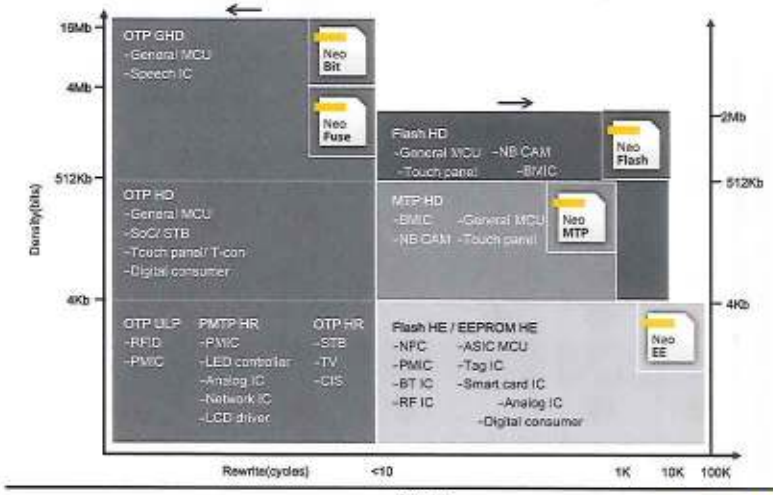
- About eMemory
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Technology Portfolio

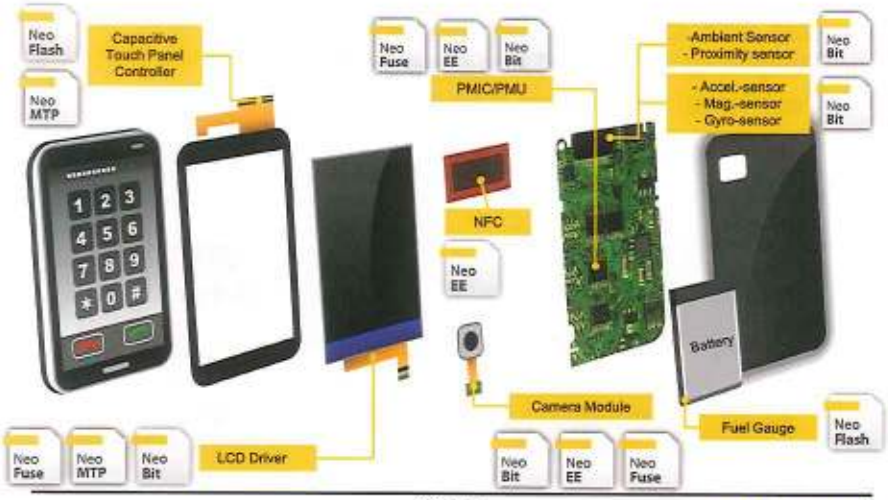


Innovative Technologies

- Wide selections of embedded NVMs for manu applications



eMemory IPs inside Smart Phone



Outline

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NVM Usage

Purpose	When			What	Why
	Programming Phase			NVM Type	Usage
	CP	FT	System/ End user		
F/W Code Storage		V	V	MTP/Flash	Store F/W code based on different models
Analog Trimming	V	V		OTP	Minimize process variations
Parameters Setting			V	Flash/EEPROM	System fine tuning or user preference setting
Encryption			V	OTP/MTP	Security or copyright content
ID Setting		V	V	OTP/MTP/EEPROM	Store product information or ID matching
Function Selection		V		OTP	Define different function organization from same bare die

Product Development



One-time storage for ID, trimming, encryption…

Multi-time rewrite for system calibration, function selection…

Why Not Adopt

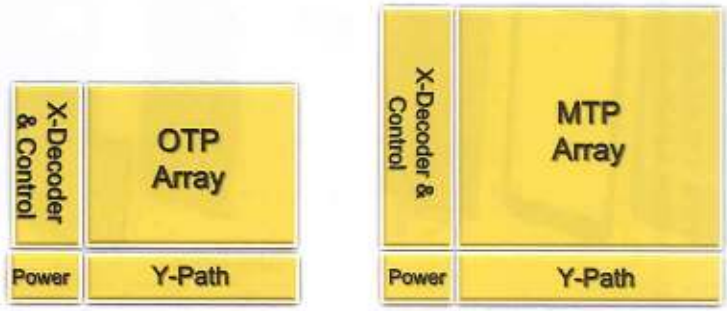
Hybrid NVM solution with customized SPEC & optimized size



Cost-effectiveness from optimized integration of NeoBit & NeoMTP

Hybrid NVM IP Concept

Cell Size: OTP is smaller than MTP
Peripheral Circuit: OTP is simpler than MTP
Test Time: OTP is less than MTP

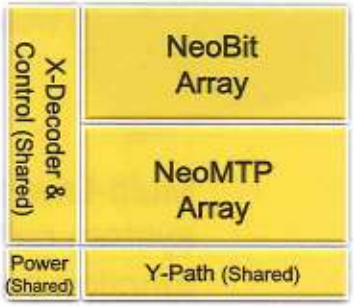


When To Use Hybrid NVM IP

Customized SPEC from customer demands

Size optimization by shared peripheral design

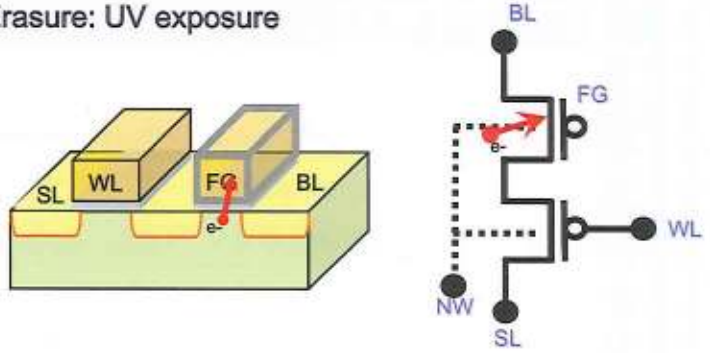
Use one simple IO and command for NVM IP…



NeoBit Technology

Programming: Channel hot electron injection

Erasure: UV exposure

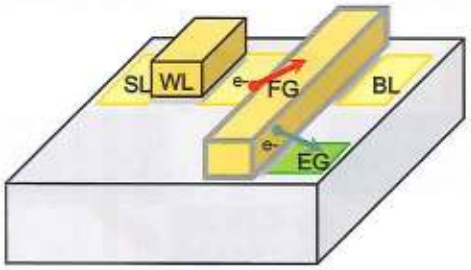


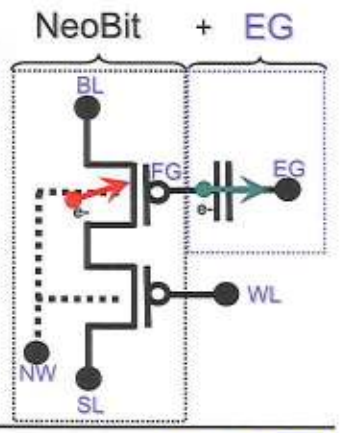
NeoMTP Technology

Programming: Channel hot electron injection

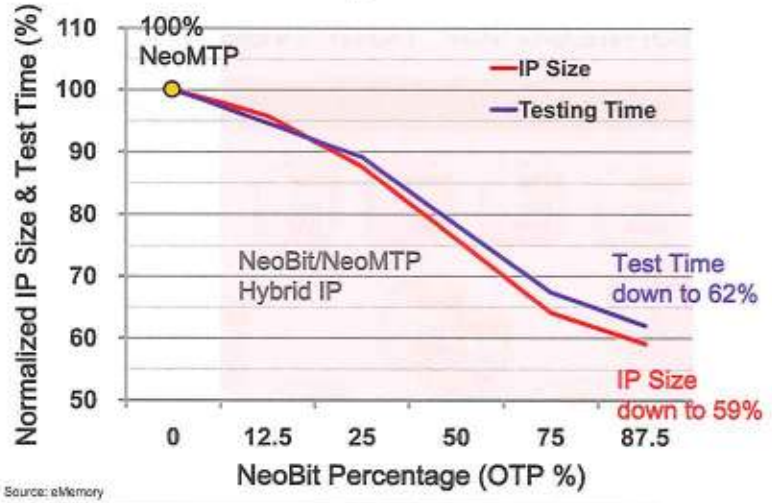
Erasure: FN tunneling ejection

NeoMTP: Electrical erasable NeoBit





Benefits from Hybrid IP



Source: eMemory

eMemory Hybrid NVM IP Solutions

- eMemory Hybrid NVM IP solutions make TSMC logic process platform more value-added



- Product development on TSMC logic platform with eMemory comprehensive & hybrid solutions make your products more cost-effective and competitive

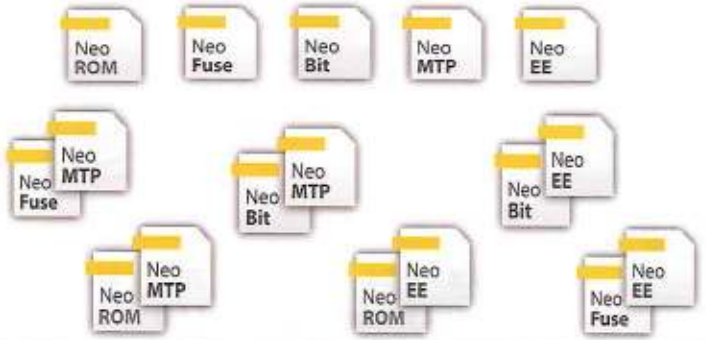


Outline

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One-Stop Service Customized for Your Needs

Comprehensive NVM solutions on TSMC logic platform

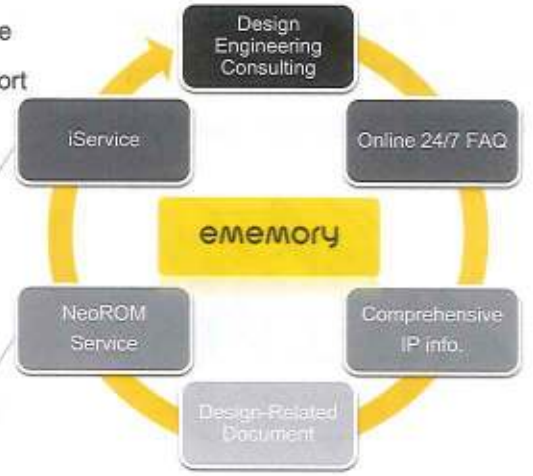


Fulfill All Your Need

- Flexible design service
- Strong technical support

› Downloadable data sheets
› Complete design kit

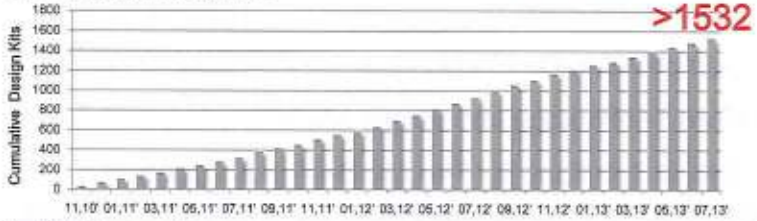
› OTP (Design) → ROM (MP)
› Reduce testing cost
› Self-certificated



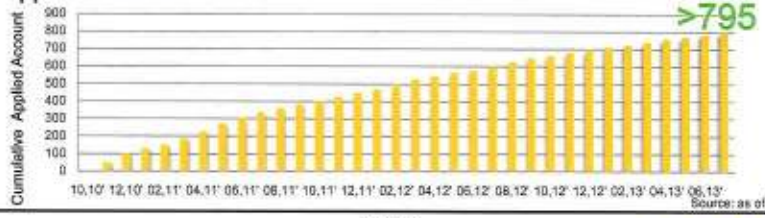
iService Performance

- Downloaded Design Kit

http://iservice.ememory.com.tw



- Applied Account



Outline

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Summary

- One-stop service for comprehensive NVM solutions on TSMC technology platform
- Logic NVM solutions: NeoBit, NeoEE, NeoMTP and NeoFuse for wide product applications
- Hybrid NVM solutions enhance logic NVM utilizations and bring more value-added on logic process platform
- Product development with Hybrid NVM solutions make your products and applications more competitive and flexible

eMemory

Embedded Wisely, Embedded Widely

Optimizing Cortex-A57 for TSMC 16nm FinFET

ARM

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

The Cortex™-A57 processor is ARM's highest performing processor, designed to further extend the capabilities of future mobile and enterprise computing applications. 16nm FinFET technology (16FF) provides the best value in speed/power optimization to meet next generation products in Networking and mobile computing applications, including smartphones, tablets and high-end SoC (System-on-Chip) devices. ARM will present a summary of the two-year collaboration with TSMC to optimize the process technology and processor implementation as they ready the ecosystem for mutual customers to implement the best ARM-based SoCs on FinFET. Topics will include discussion of the first Cortex-A57 on 16FF silicon results, methodologies for PPA optimization employed in a subsequent Cortex-A57 tape out, and how customers can leverage this knowledge in their SoC designs.

Optimizing Cortex®-A57 Processors for TSMC 16nm FinFET

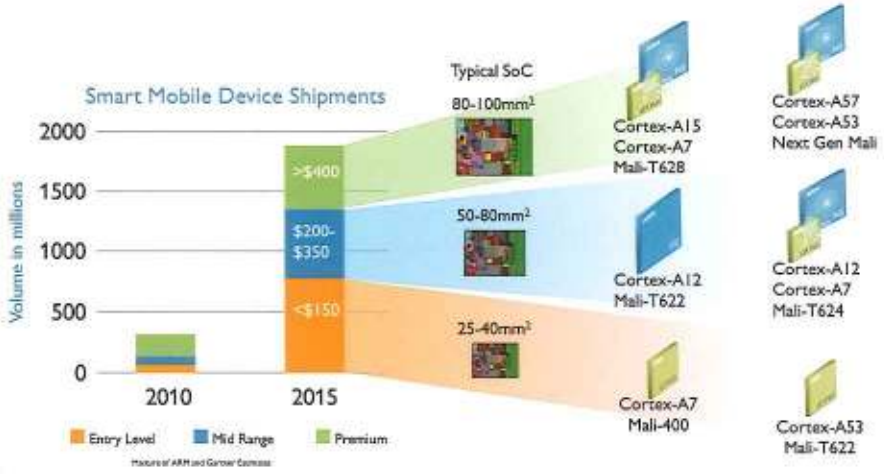
Tim Whitfield
Director, Hsinchu Design Center
Hsinchu, Taiwan

Modern Mobile Experience

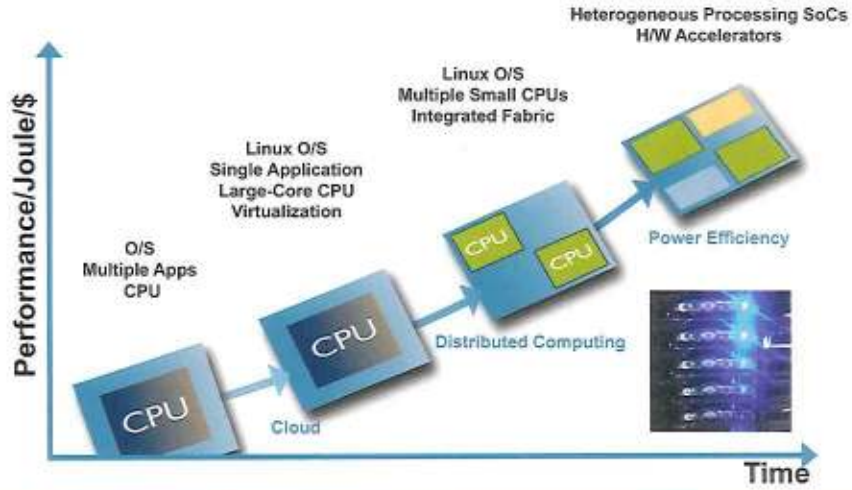


More Than Just the Phone

One Size Does Not Fit All

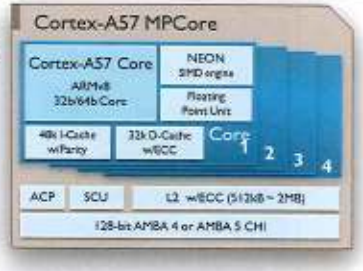


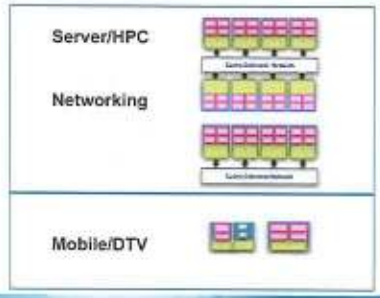
Servers Will Mimic Mobile SoC Evolution



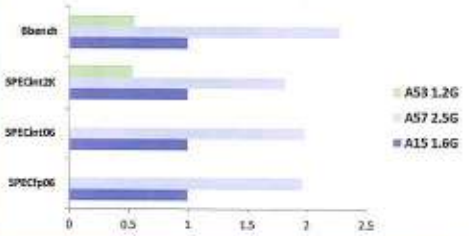
Cortex-A57 Highest Performance ARMv8 core

- **Power Efficient Performance**
 - Highest performance/watt ARM core
 - 64bit architecture, virtualization and RAS features
 - Multi-core scalability up to 64 cores (w/CCN)
- **big.LITTLE**
 - Companion to Cortex-A53 LITTLE
- **Applications**
 - **Enterprise/Networking/Storage**
 - Premium **Mobile**

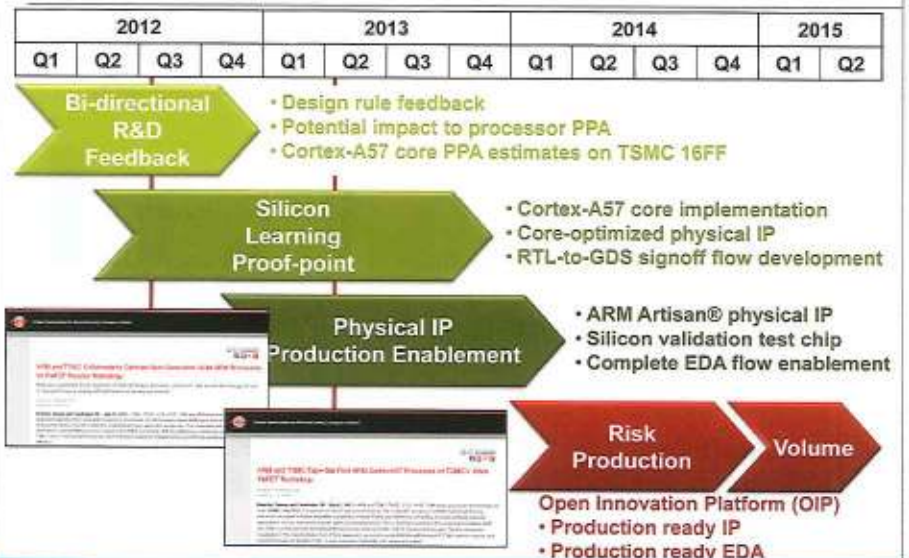




Cortex-A57 Highest Performance AT-SPEED Cortex-A Processor

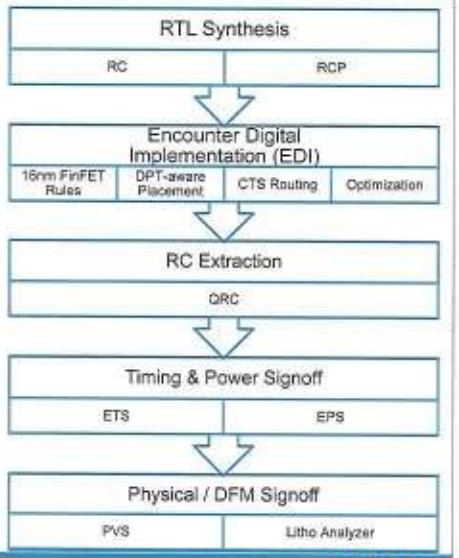


ARM-TSMC Collaboration Model



The Value of Collaboration

- TSMC, Cadence, and ARM engineers co-located in ARM's Hsinchu Design Center
- Combined expertise covering all eco-system elements
 - Cortex CPU architecture and implementation
 - Physical libraries
 - Process and design rules
 - Leading edge tools and flows
- Access to Cadence R&D
 - Fast turn around debug
 - FinFET tool enhancements



Readying the Ecosystem – Phase 1

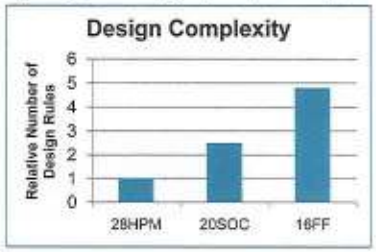
Goal: Ensure ecosystem readiness of ARM processors on TSMC 16nm FinFET process technology

- Phase 1 Objectives
 - Early process engagement through ARM R&D silicon group to gain understanding of FinFET process technologies
 - Implementation learning and feedback to ecosystem partners – process technology, library development, and EDA teams
 - Silicon proof point of ARM processors on FinFET using RTL-to-GDS signoff methodologies

ARM cadence tsmc

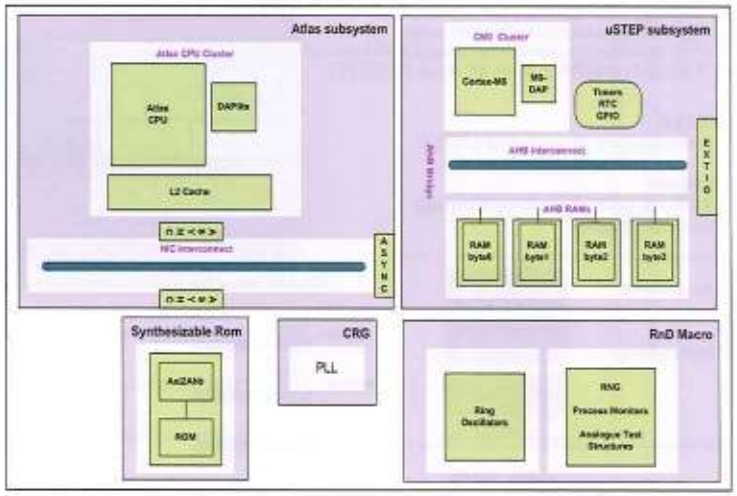
Project Challenges

- Dynamic design environment with rapidly changing IP, design rules and EDA tools
 - Limited implementation choices
 - Metal stack, Vt, library
 - Increased design rule complexity coupled with rapid iteration
 - Large "real" design – long tool run times
 - New design requirements imposed by finFET process



- Aggressive schedule with concurrent changes to process technology, processor RTL, physical IP, and EDA flow

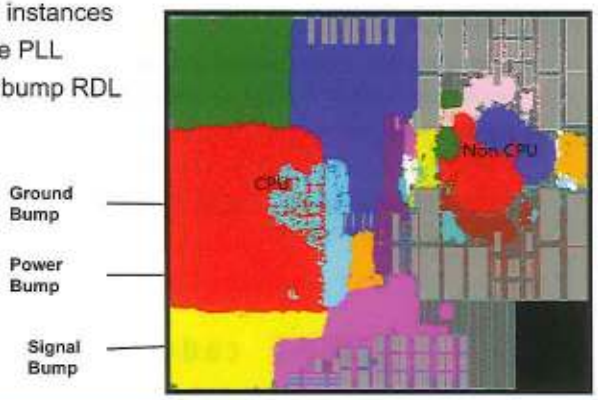
Phase 1 Logical Design



Alligator Test Chip Logical Architecture

Phase 1 Physical Design

- Top level and CPU floor plans
 - Cortex-M0 sub-system: 86K instances
 - Cortex-A57 sub-system: 2.85M instances
 - RAM: 115 macro instances
 - High performance PLL
 - Flip chip I/O and bump RDL



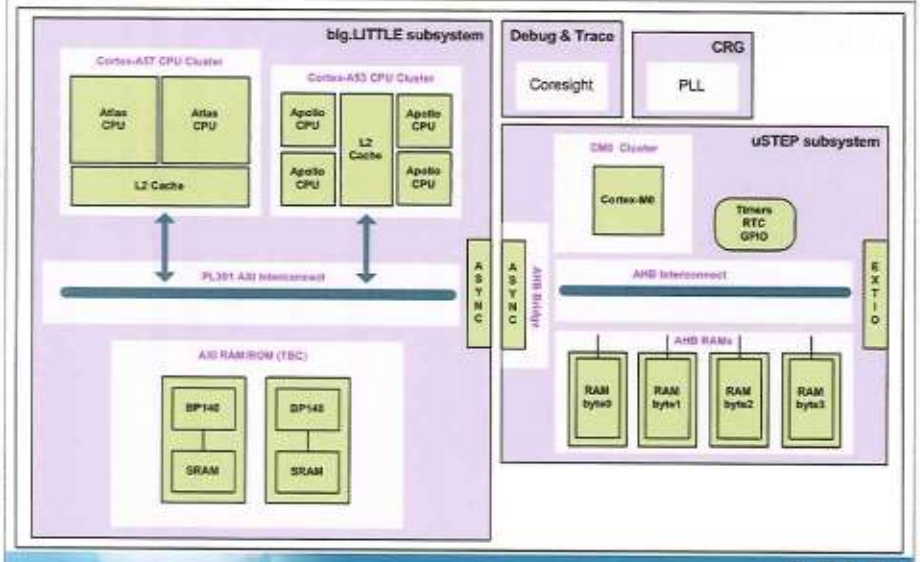
Readying the Ecosystem – Phase 2

Goal: Ensure ecosystem readiness of ARM processors on TSMC 16nm FinFET process technology

- Phase 2 Objectives
 - Continued collaboration with ecosystem partners
 - Optimization of ARM big.LITTLE solution on N16FF
 - Configurations and PPA targets for high end mobile applications
 - Physical library development support
 - Lead partner engagements and knowledge sharing with partners
 - Demonstrate ecosystem readiness for ARM-based SoCs

ARM cadence tsmc

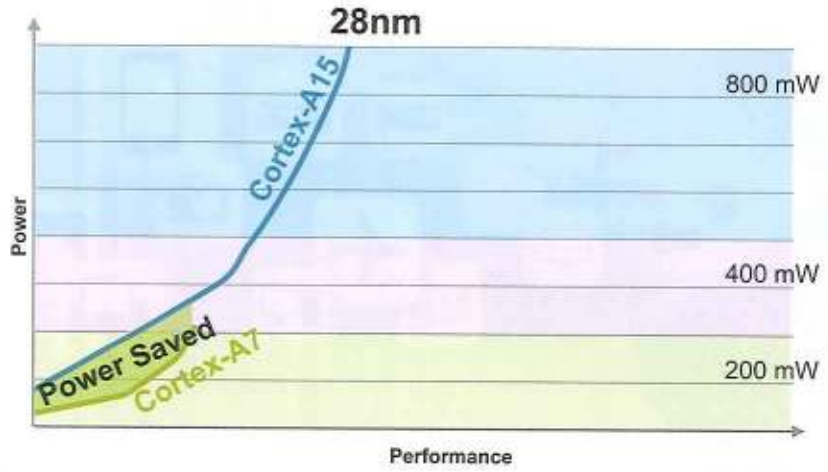
Phase 2 Logical Design



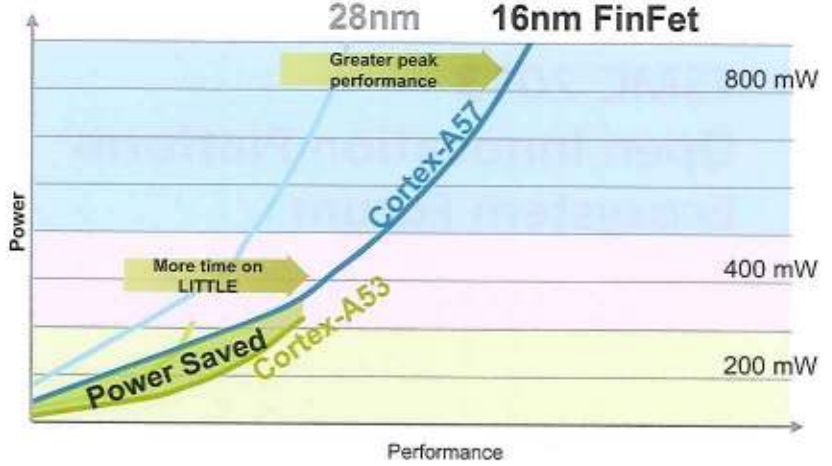
Current Status

- Phase 1 silicon back and …
- Phase 2 silicon tape-out November 2013
- Lead Partner engagements underway with ARM Artisan® Physical IP platform
- Continued optimization for mobile and enterprise through ARM POP™ IP development for Cortex A57 and Cortex A53

Future-proof Leadership with big.LITTLE



Future-proof Leadership with big.LITTLE



Kilopass Expanding Product Roadmap for TSMC Advanced Process Nodes

Kilopass

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

One-time programmable (OTP) anti-fuse technology provides tamper-resistant and reliable non-volatile memory storage by causing gate oxide breakdown (BVox) in a standard logic CMOS transistor. Last year, Kilopass developed a patented new technology called vertical crosspoint memory (VCM) that boosts OTP anti-fuse storage density 4-fold using a novel logic CMOS transistor that requires one additional minor manufacturing step to build. Because anti-fuse OTP NVM IP uses standard logic CMOS transistors to store data, the memory scales to each new process node with no technology roadblocks even with FinFet and other 3D device architectures. This presentation will describe Kilopass' OTP roadmap for all variants of TSMC's process nodes from 180nm to 28nm, where Kilopass IP is fully qualified. It will then detail our designs on TSMC 20nm and highlight our design progress on TSMC 16nm FinFet.

Kilopass

Kilopass Expanding Product Roadmap for TSMC Advanced Process Nodes

Harry Luan, CTO, VP of Research & Development
Kilopass Technology Inc.

Outline

- About Kilopass technology
- Overview of Kilopass OTP cell technology
- Vertical Crosspoint Memory expanding OTP applications
- Progress porting VCM to TSMC 55HV
- Kilopass eNVM technology roadmap
- Kilopass OTP technology scaling to 20nm and beyond
- Summary

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Kilopass

Kilopass Corporate Overview

Logic NVM Innovator	• Kilopass founded 2001, standard CMOS possible, Gox breakdown < BVj • Conceived at the right time, when 0.18um came to market
Proven & Patented Embedded NVM in CMOS	• 58 patents granted/pending, including fundamental patents on 1T, 2T, and 3.5T anti-fuse • 0.18um to 40nm qualified and in production; 1st to demonstrate reliability in 28HKMG; T/O-ed 20G, 20SOC
Broadly Adopted	• 150+ customers • 400+ design ins • 2 billion+ units shipped
Key Markets	• Analog: audio tuners, clock chips, PMU, LED lighting • Automotive: DSP, I/O connectivity, micro sensor systems • Mobility: PA, RF transceiver, baseband, DDI, CIS • Consumer: media & app processors, PC multimedia
Key Usages	• Small capacity (< 256Kb): Configuration, yield recovery, security keys, code patching of ROM • Large capacity (> 512Kb) : Code storage

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Kilopass

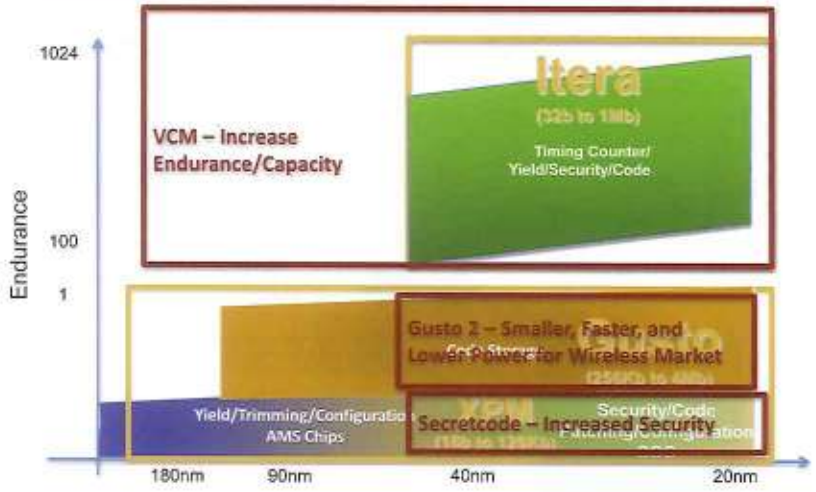
Kilopass Product Offering: XPM, Gusto, and Itera



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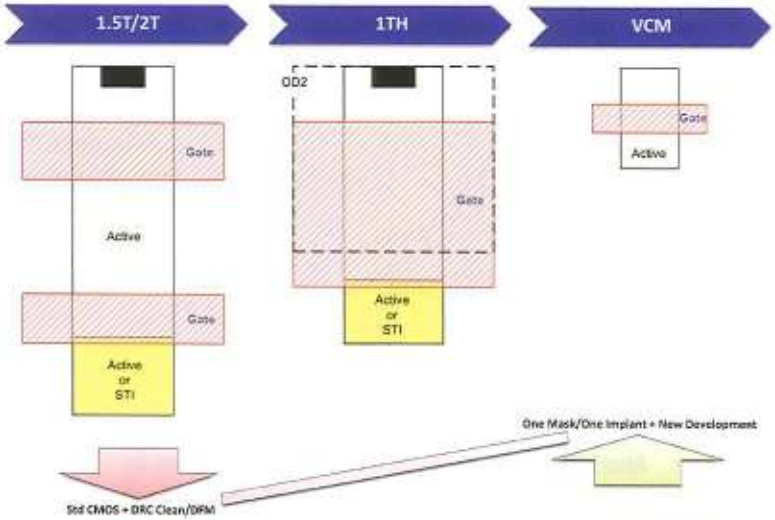
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Product Roadmap Expansion



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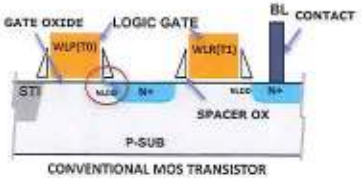
Enabling Antifuse Cell Technologies from 2T to 1TV VCM



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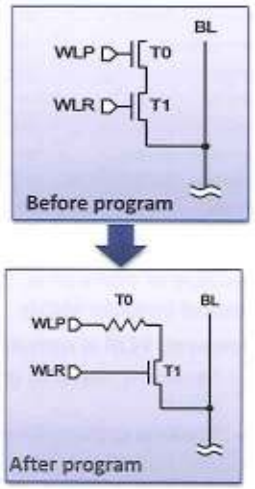
2T Bitcell Operating Principle

Cell Cross Section



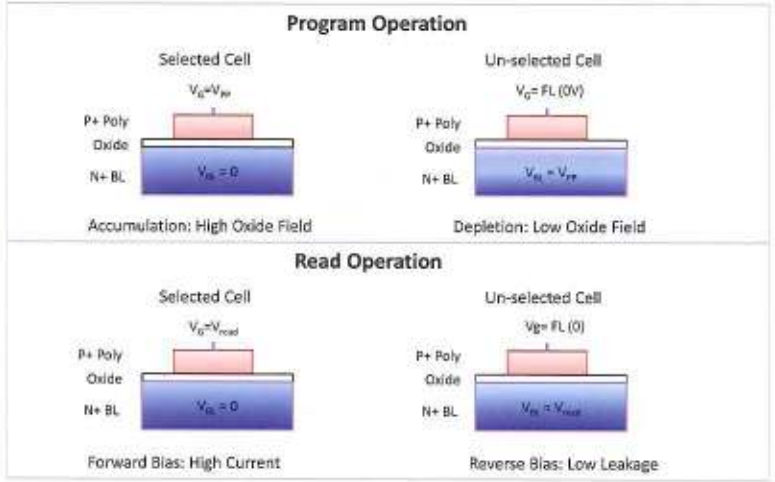


2T Cell Schematic



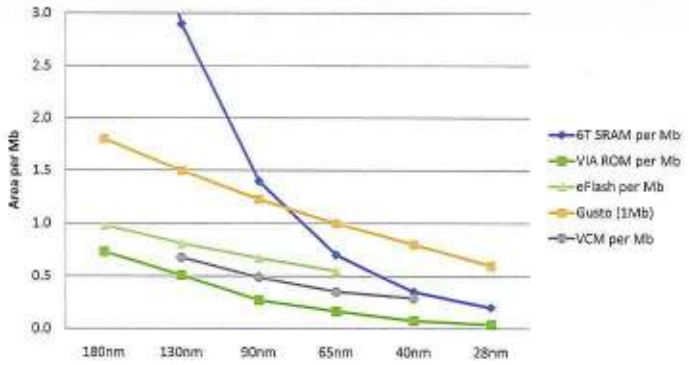
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VCM Bitcell Operation Principle



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Comparing VCM to Other Embedded Memory

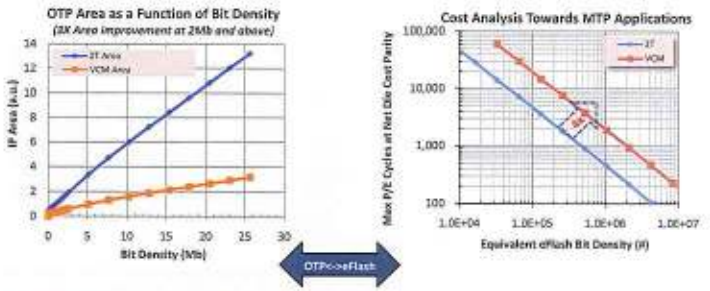


- **Best fit in replacing eFlash**
- **Also SRAM in mobile application for long stand-by**
- **May substitute ROM in customer-specific products**

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Kilopass VCM – 4x Area Reduction Vs. Conventional OTP NVM



2T does not meet VCM Area Requirement
- 2T bit cell architecture doesn't meet Numera area requirement
- The technology can only serve a small percentage of eFlash market – 1k cycles up to 256Kb or 1Mb for less than 500 cycles (10% sector update)

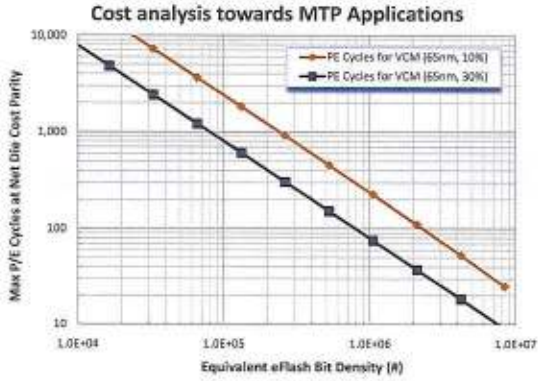
1TH is only good for <2X area improvement
- 1TH needs tighter overlay control although it does not require extra masking/process
- 1TH can only give ~2X area improvement due to smaller OEC area

VCM gives >3X area reduction above 2Mb
- VCM gives the required >3X area reduction for eFlash replacement
- The extra mask/implant required for VCM is similar to regular n-well implant.

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Using VCM in eFlash MTP Applications



- **Cost equivalence analysis at 65nm, 30mm2 SOC with 10% or 30% re-write each time**
- **Parameterized model can model 180nm – 65nm (no 40nm eFlash)**

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VCM 90nm Analysis by MCU IDM

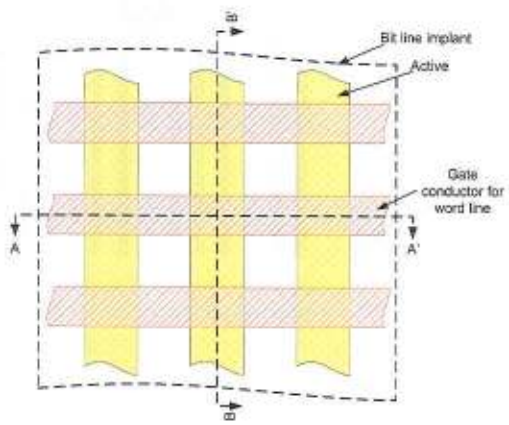
128KB Specification	eFlash	VCM	Note
Modularity to CMOS Logic	NO	Yes	IP re-design
Roadmap migration	Difficult	Easy	
Extra Masks	+8 – 10 layers	+ 1 layer	25% + savings with VCM
Area (mm^2)	2.0	0.8 – 2.4	Endurance dependent
Endurance	10K	1 - 100	4KW/write
Program time per byte (µs)	50	16	
Typ Active Power (mW/MHz/32 bits)	2.75	0.2	VCM lower active power
Security Lock	SW only	Yes, HW	Built in security with VCM

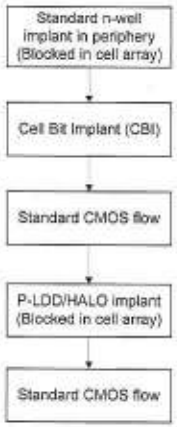
- **Because of endurance, VCM not likely to replace eFlash in traditional, general purpose MCUs**
- **However, VCM is compelling in two other areas**
 - Modularity: migration of IP from baseline CMOS to include eNVM without porting efforts
 - Roadmap to 65nm/40nm with advanced digital integration

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VCM Technology – Array Layout and Process Flow

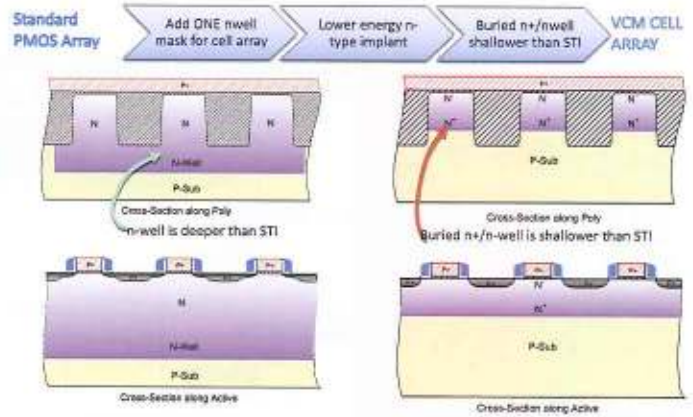




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VCM Bit Cells – CMOS-compatible with Only One Additonal Mask for a nwell-like Bitline Implant



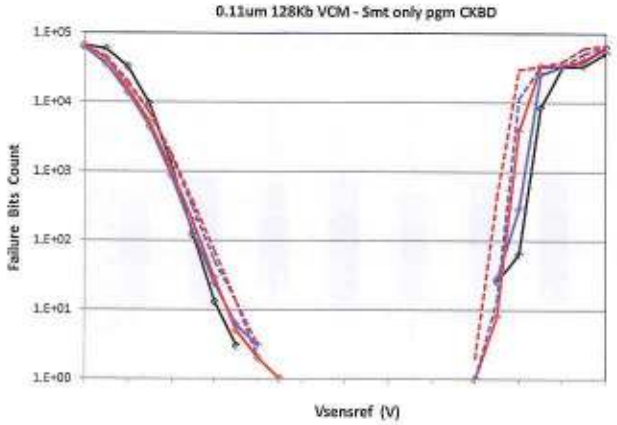
- The VCM bit cell is similar to PMOS except that n-/n+ doping profile is shallower than the regular n-well (and STI) so that n+ bit lines are not shorted to each other
- The extra mask is non-critical and used before or after the regular n-well implant. No additional thermal annealing is needed.

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110nm VCM Review – 128Kb Summary Characteristics

- **Checkerboard programmed 128Kb show robust programming window across different BL implant splits**



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VCM Technology for Both Logic and HV Processes

ITEM	65HV/55HV 1.2V/6V
Density	8Mb
Architecture	VCM
Programming bus width	X32
Read bus width	X32
tACC	40ns
Charge Pump or VPP	Vpp
Programming Voltages	VDDIO= 2.3 ~ 4.8V, VDD=1.2V +/-10% , Vpp= 6.5 +/-0.25V
Read Voltages	VDDIO= 2.3 ~ 4.8V, VDD=1.2V +/-10%
Programming Temperature	0°C - 85°C
Read Temperature	-40°C - 85°C
Metal Layers	5LM
Area (mm2)	3.2
Programming Time	40us/word
Standby Current (typ)	1uA
Active Current (typ) @10MHz	4.5mW
Programming Current	<10mA
Features	emulated MTP (example: 1Mb, 20% rewrite, 35 cycles)

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Kilopass eNVM Roadmap



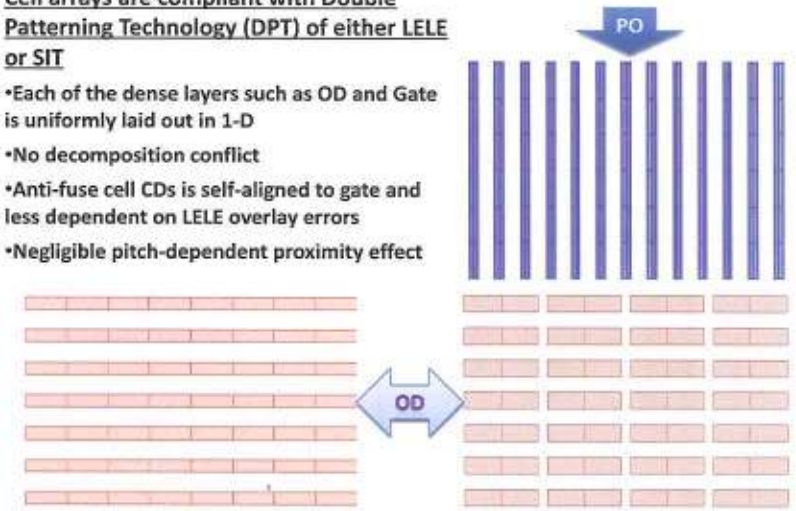
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Kilopass OTP scales very well to 20nm and beyond

Cell arrays are compliant with Double Patterning Technology (DPT) of either LELE or SIT

- Each of the dense layers such as OD and Gate is uniformly laid out in 1-D
- No decomposition conflict
- Anti-fuse cell CDs is self-aligned to gate and less dependent on LELE overlay errors
- Negligible pitch-dependent proximity effect

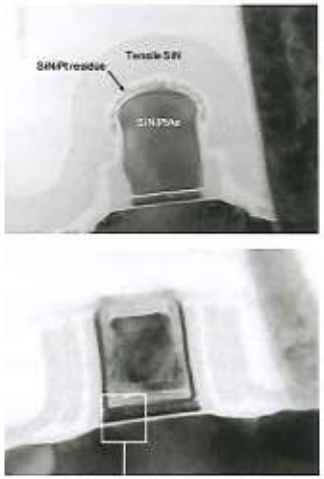


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Excellent Manufacturability, Scalability, and Reliability on HKMG

- Cell array uses foundry standard nMOSFETs only
- No non-critical mask features inside memory array
- Fully compliant to DFM rules and independent of HKMG integration scheme
 - HKMG First
 - HK First/Metal Last
 - HKMG Last
- Excellent reliability demonstrated on 28nm and scalability to 20nm and beyond, planar or 3D



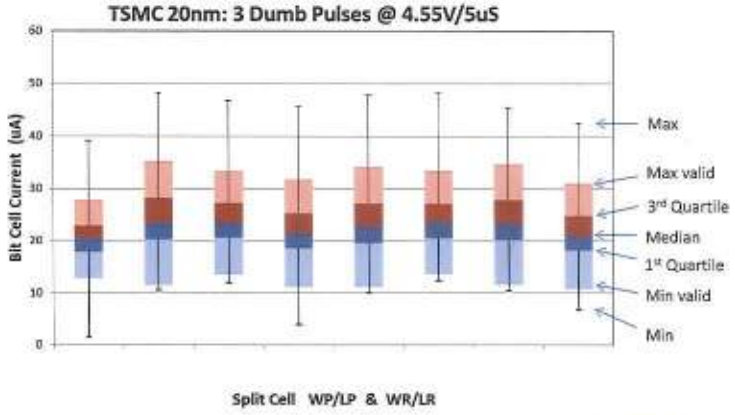
(James, ASMC 2012)

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8kb OTP on 20SoC – Programmable Array Split Cells

- Like that shown for 20G, good programmed cell current across different cell dimensional splits
 - W=0.08~0.14-micron, Lwp and Lwr=26~30nm

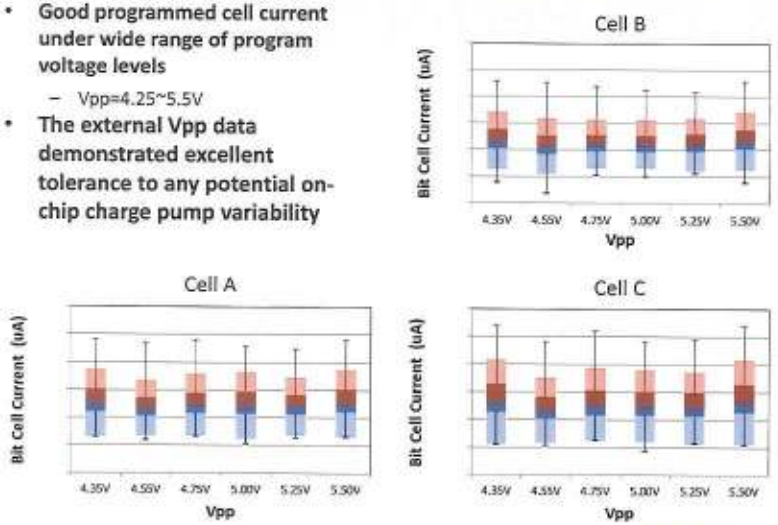


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8kb OTP on 20SoC – Programmable Array Split Cells

- Good programmed cell current under wide range of program voltage levels
 - Vpp=4.25~5.5V
- The external Vpp data demonstrated excellent tolerance to any potential on-chip charge pump variability

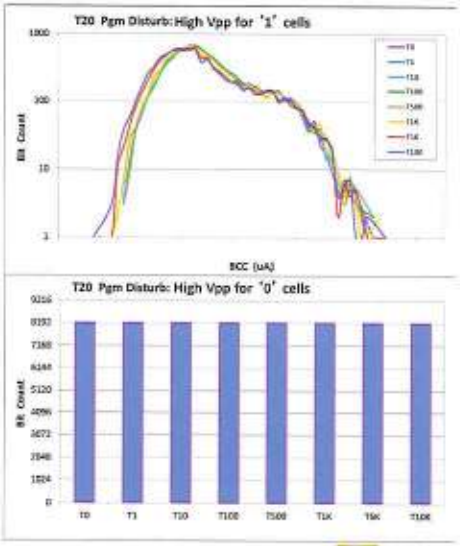


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8kb OTP on 20SoC – Very Robust Immunity to Program Disturbance

- 16Kb array was first programmed into checkerboard patterns and then stressed at the worst-case Vpp and time of 10K pulses
 - No statistically significant change observed for programmed cell current
 - Un-programmed cell leakages are still below tester resolution

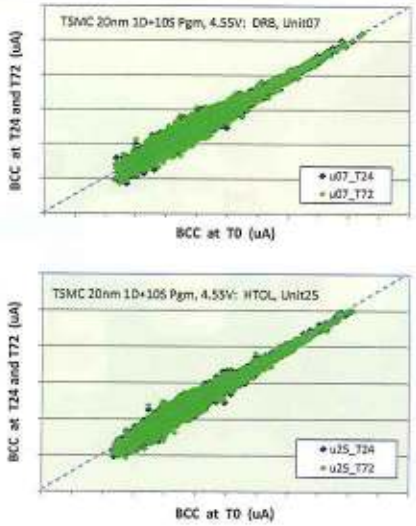


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8kb OTP on 20SoC – DRB and HTOL Show Excellent Reliability

- 16Kb array first programmed into checkerboard patterns using 'Smart' programming with a verify Icell
- Data retention bake was done at 150C unbiased
- HTOL done at 125C with read voltage acceleration
- A cell current change of ~±2uA is observed at 24Hr for cells with low to medium initial current.
- No statistically significant change between 24Hr and 72Hr. This is true for both DRB and HTOL
- Results show that OTP on 20SoC should have the same high reliability as OTPs already demonstrated on 28nm processes



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Summary

- The leader in embedded OTP memory, Kilopass offers comprehensive solutions on TSMC processes 180nm to advanced 28nm and below
- Kilopass' anti-fuse 2T OTP memory performs effectively and reliably on all TSMC poly, HKMG, and HV processes
- Kilopass VCM 4x density OTP memory is being qualified on TSMC 55HV process
- Kilopass OTP memories are first to achieve HTOL and HTSL qualification on TSMC's 28HKMG & 28LP processes
- Kilopass' OTP technology has demonstrated excellent performance and manufacturability on TSMC's 20nm HKMG process
- Kilopass' OTP technology continues scaling to CMOS process nodes 1x node and beyond

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The Impact of FinFET Technology on Physical IP Development, Design Styles and Performance

Synopsys

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

In order to fully realize the advantages of FinFET devices, physical IP must follow the same trajectory that has benefited digital design. That is: scaling, lower power consumption and higher speeds. To achieve this, analog/mixed-signal development techniques and design styles have to be re-created and implemented with very close foundry co-operation.

From a designer's perspective whether the technology is planar or FinFET, the parameters of interest are the same: transistor gain, output conductance, transition frequency, matching, noise and device aging – their target is to achieve performance whilst meeting the system-on-chip constraints of power and area. In terms of new analog/mixed-signal design styles, FinFET's provide: an improved sub-threshold and short channel behaviour, associated with low leakage currents; very low output conductance due to the lower channel doping providing an advantage in terms of instrinsic gain; better matching behaviour; and, the metal gates eliminate poly depletion effects. For SRAMs the higher gate capacitance means that the fan-out needs to be adjusted, the lack of body effect requires that the transistors are adjusted in series for pull-up and pull-down. Although not strictly related to FinFET's, high-k dielectrics can be used to reduce gate tunneling currents but this increases flicker noise or reduces mobility. An interesting aspect to this is that designers will leverage FinFET properties to invent new circuits in the future.

This presentation will highlight: 1) the FinFET transistor characteristics that make them different for phyiscal IP design compared to planar devices; 2) the impact FinFETs have on existing circuit designs and layout topologies for DDR, USB, PCI Express and foundation IP; 3) methodology that incorporates advanced process qualification vehicles; 4) an integrated test, repair and diagnostics solution that supports repairable or non-repairable embedded memories; 5) close co-operation with TSMC through the Open Innovation Program.

The Impact Of FinFET Technology On Physical IP Development, Design Styles and Performance

Navraj Nandra
October 2013

SYNOPSYS®
Accelerating Innovation

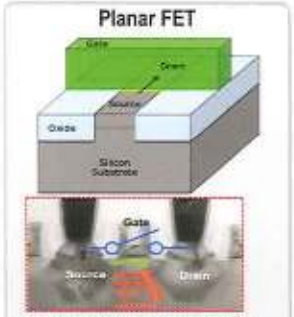
Agenda

- FinFET And Planar Devices
- Impact Of FinFETs On Circuit Design
- FinFET Defect Detection
- Advanced Qualification Methodology
- Summary

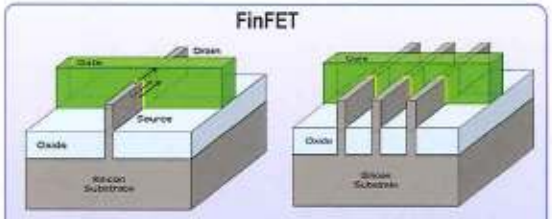


How FinFETs Work

Field Effect Transistors: Gate(s) Control Of The Channel



Single gate channel control is limited at 20-nm and below



"Multiple" gate surrounds a thin channel and can "fully deplete" it of carriers. This results in much better electrical characteristics.

FinFET Transistor Characteristics

Output Curves: Voltage (V), Current (I)







1. Planar and FinFET
2. FinFET Gate Length
3. Number of Fins

Control through number of fins and gate length

FinFET Advantages & Considerations

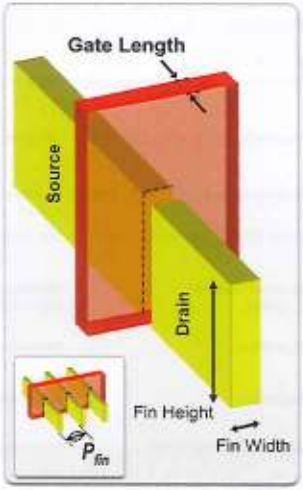
Improved Characteristics; Impacts Circuit Design

Advantages

- Lower leakage
- Less V_t variability
- Less variability
- Lower operating voltage

Additional Considerations

- Quantized widths
- No body biasing
- Higher parasitics
- Self-heating
- ESD can be an issue
- Degradation and aging



Agenda

FinFET And Planar Devices

Impact Of FinFETs On Circuit Design

FinFET Defect Detection

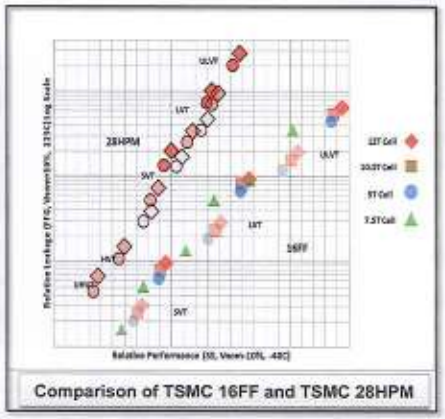
Advanced Qualification Methodology

Summary

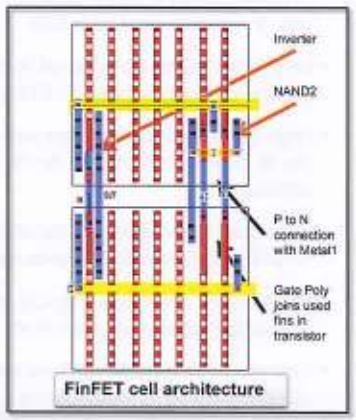


FinFET Impact On Logic Libraries

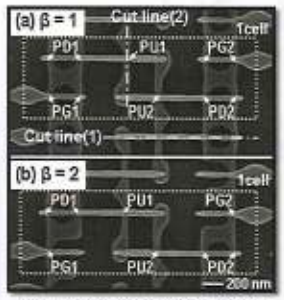
Of Tracks Less Impact; New Cell Architectures



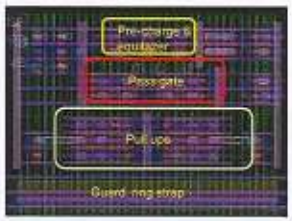
Comparison of TSMC 16FF and TSMC 28HPM



FinFET cell architecture



Source: Kawasaki et al, 2006 Symposium on VLSI technology Digest of Technical Papers



Synopsys FinFET Sense AMP

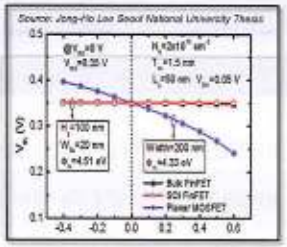
FinFET SRAMs
The Good News

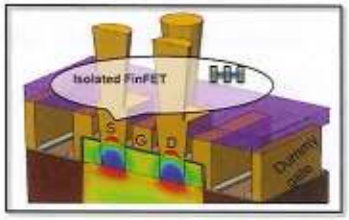
- Higher performance and lower leakage compared to planar
- Operates at lower Vdd than planar
- Good static noise margin (SNM) at low Vdd
 - Can achieve decent noise to signal ratio (with a β=2 for example)
 - Good (low) variability
 - Narrower read and write margins than planar

FinFET SRAM Challenges

Quantized Beta; New Layout Effects

- The β ratio is a quantized number thus fine-tuning β is not possible
 - Challenge for read and write margins
 - Requires assist circuitry
- Body-bias techniques are not efficient – new techniques needed
- Realizing long channel devices is litho driven (DP vs. spacer) with limited options
 - Stack short channels in series
 - Manipulation of spacer (very limited)
 - Multi-Fin pitch
- Layout effects on devices critical (lonely FinFET phenomena)





SRAM Assist Schemes Survey

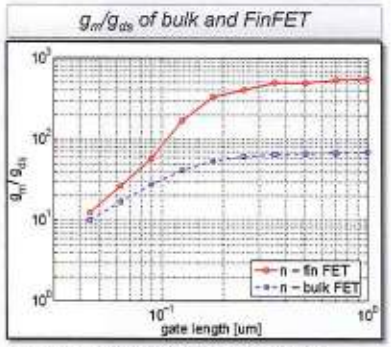
Multiple Assist Techniques Deployed

TECHNIQUE	HELPS	CONCEPT	COMMENTS
Constant negative-level write buffer (CNL-WB)	Write margin	BL-level adjustment	Suitable for memory compilers
Dynamic power supply (column based)	Read and write margins	SRAM cell voltage to be switched dynamically based on the actual read, write	Various techniques, some need IO VDD source . Can have dummy read issues
Negative bit-line capacitive coupling	Write margin	Improves pass-gate transistor drive compared to pull-up	No dummy read problems, No area/ power penalty, No external VDD needed.
Adaptive dynamic word-line underdrive	Read margin /Write margin	Forward bias/ reverse bias pull-up for higher / lower drive	Each done separately at the expense of the other margin
Sense AMP bit-line amplification	Read margin	Provides full BL amplification to half-selected columns. Full BL amplification	Significant overhead cost
Word-line lowering	Read margin	Weaken pass-gate transistor drive	Bad for power
BL pulsing	Read margin	Improves the discharge rate of the low-node of the cell	Deteriorates writability
WL pulsing	Read margin	Provides data recovery by writing back the original data prior to the disturb.	Deteriorates writability
Dual Supply	Read margin		Has power savings angle in addition to read margin improvement
RMW (Read Modify Write)	Read margin	Use pre-column sense amp. All cells are read first and re-written	Sense amp timing is critical

Impact On Circuit Schematic Style

USB, DDR, PCI Express, Analog IP

- PMOS/NMOS drive strength similar
- Device matching better than planar (although variation of Tox, εox) WF along the fin height)
- W/L mapped to L and # fins
- Strict binning of device sizes
- Quantized devices → stacked devices → increases parasitics → new designs needed for high speed blocks
- Aging simulation is important, NBTI dominates PBTI



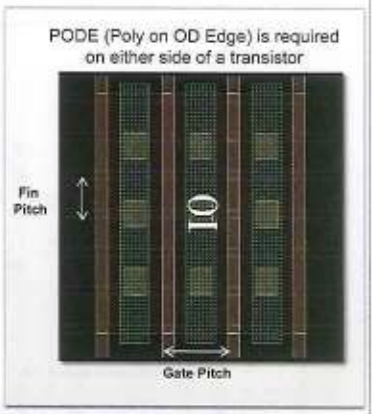
Designers care about g_m, g_{ds}, F_t, F_{max}, matching, noise for SoC PPA

Include process information to create optimized FinFET schematics

Impact On Layout Style

USB, DDR, PCI Express, Analog IP

- Smaller devices (same current), devices get hot → need to deal with EM
- New tools being developed to speed the design process related to EM and IR
- High speed divider causes self-heating (local thermal effects) → more vias and diffusion
- Significantly increased rule count → DRC complex and time-consuming
- Metal stack selection impacts routing orientation and pitch selection
- Increased R in metal routing mandating need for full RCC simulations

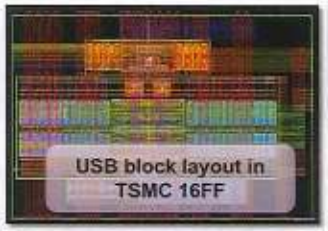


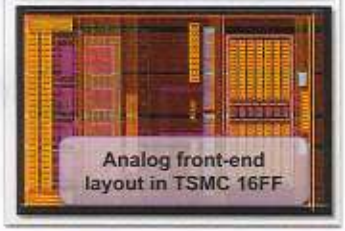
Start layout and metallization earlier in the design process

Impact On Development Style

USB, DDR, PCI Express, Analog IP

- Lower power supply (0.8 V for TSMC 16FF)
- Increased capacitance density
- High voltage tol. big concern, reduced breakdown voltages impacts USB
- Increased requirement of power-aware settings in .lib files & power gating on unused circuits
- Device/interconnectivity complexity, increases CPU load
- In-house ESD expertise is a must
- New design flows developed using Synopsys AMS tools
- Silicon to HSPICE/Finesim correlation successful on 20-nm





New design styles, EDA tools implemented in-house to meet IP specs

Agenda

FinFET And Planar Devices
Impact Of FinFETs On Circuit Design
FinFET Defect Detection
Advanced Qualification Methodology
Summary



Defects In FinFET Transistors

Resistive shorts between fins



Resistive opens on fins



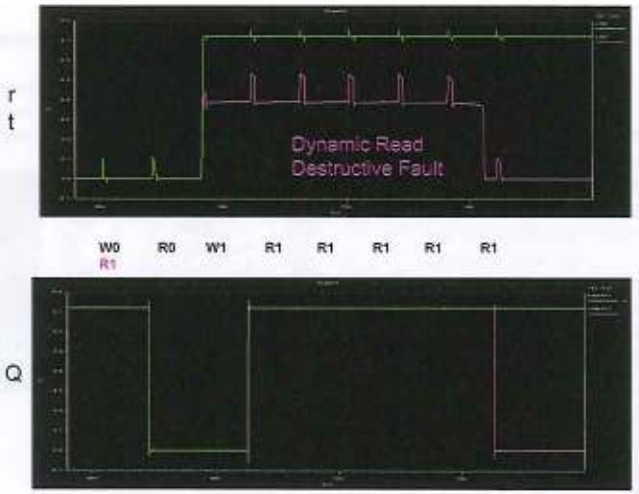
Performed comprehensive fault modeling of **FinFET specific defects** involving all SRAM cell transistor nodes and fins

(ex: resistive Fin shorts, Fin channel opens, Fin channel stuck-on, Gate-Fin shorts, etc.)

In addition to traditional process variation and spot defects

Synopsys Defect Injection Methodology

Example: FinFET Resistive Open Defect Df11



Full FinFET Defect Detection For Memory Test & Repair

Development flow to detect FinFET cell defects using an advanced test engine

Step 1. Defect injection and fault modeling
Step 2. Test sequence and optimal PVT identification
Step 3. Test algorithm synthesis
Step 4. FinFET Enhanced SMS 5

STAR Memory System 5

New addressing mechanisms: H1 addressing, ping-pong
Fully programmable background patterns
Programmable test operations: concurrent operations
Stress conditions: voltage, temperature, frequency

Agenda

FinFET And Planar Devices
Impact Of FinFETs On Circuit Design
FinFET Defect Detection
Advanced Qualification Methodology
Summary



Designing IP In FinFET Technology

Deeper Link Between Layout, PPA, TSMC Collaboration

Semiconductor Process Requirements

- WPE
- LOD
- OSE
- PSE
- PO.DN.15
- Pattern Density Effect
- OPC (Optical Proximity Check)
- GDA (Gross Die Advisor) Criteria
- MFU (Mask Field Utilization) > 80%
- DFM LPC (Layout Patterning Check)
- HCI (Hot Carrier Injection) Effect
- Dummy OD (DOD) Rules
- Dummy Poly (DPO) Rules
- SM (Stress Migration)
- NBTI
- PBTI
- PSM
- RTO

PPA Requirements For Physical IP

TSMC 20-nm silicon experience is a stepping stone to FinFET:

- New methodology using process qualification vehicles with early design kits
- Provides designer DPT & RDR experience



Technology Assessment Chip

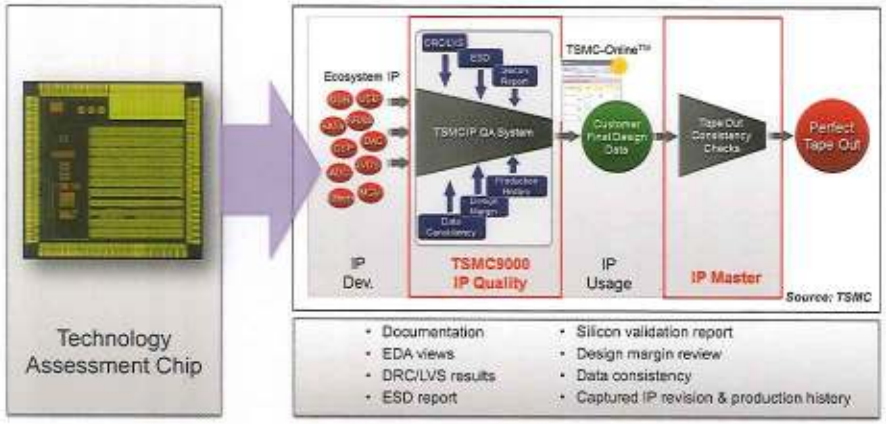
DesignWare IP for TSMC 16FF

DesignWare IP	Design Kit I Pre v1.0	Design Kit II (After v1.0)
Standard Cells	●	●
Memory Compilers	●	●
DDR3/LPDDR2 PHY	●	●
DDR3/DDR4/LPDDR4 PHY	●	●
USB 2.0 OTG PHY	●	●
USB 3.0 PHY	●	●
PCIe 1.1, 2.0, 3.0 PHY	●	●
MIPI PHY		●
SATA II/III PHY	●	●
HDMI Tx/Rx PHY		●

● Under Development

Synopsys and TSMC Collaboration

A Partnership For FinFET Physical IP Success



- Documentation
- EDA views
- DRC/LVS results
- ESD report
- Silicon validation report
- Design margin review
- Data consistency
- Captured IP revision & production history

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Agenda

- FinFET And Planar Devices
- Impact Of FinFETs On Circuit Design
- FinFET Defect Detection
- Advanced Qualification Methodology
- **Summary**



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Summary

The Impact Of FinFET Technology On Physical IP

- **Development**
 - Advanced process qualification vehicles, co-operation through TSMC OIP is a must
 - 20nm silicon experience was a stepping stone to FinFET
 - Created a new flow to detect FinFET cell defects using an advanced test engine
 - CPU load increases significantly to verify complex design rules
 - EM/IR/ESD expertise required in-house
- **Design styles**
 - Designers care about the same parameters (gm, gd, Ft, Fmax, matching, noise) in planar or FinFET to get performance while meeting the SoC constraint of power, area
 - Process information included to create optimized FinFET schematics
 - Start layout and metallization earlier in the design process
 - New design styles and EDA tools implemented in-house to meet IP specs
- **Performance**

 → Improvements in matching & less device variability but quantization, high voltage tolerance, increased parastics required new circuit architectures to meet PPA

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ARM POP IP: Accelerating Time-to-PPA in Mainstream Mobile

ARM

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

SoC design teams continue to see increases in design complexity, power management method, and time-to-market pressures. ARM POP IP is co-developed with the Cortex-A series processor cores targeting specific TSMC process technologies. Leveraging deep architectural knowledge and close collaboration with TSMC the POP IP provides optimized physical IP, reference configurations, and implementation knowledge to achieve performance and power targets in a predictable time-to-market. ARM will present an overview of its POP implementation solutions targeting mainstream mobile SoCs leveraging the Cortex-A12 and Cortex-A7 processors on TSMC 28nm high performance (HPM) and low power (LP/LP+) process technologies to help designer's achieve their SoC objectives.

ARM POP™ IP

Accelerating Time-to-PPA in Mobile

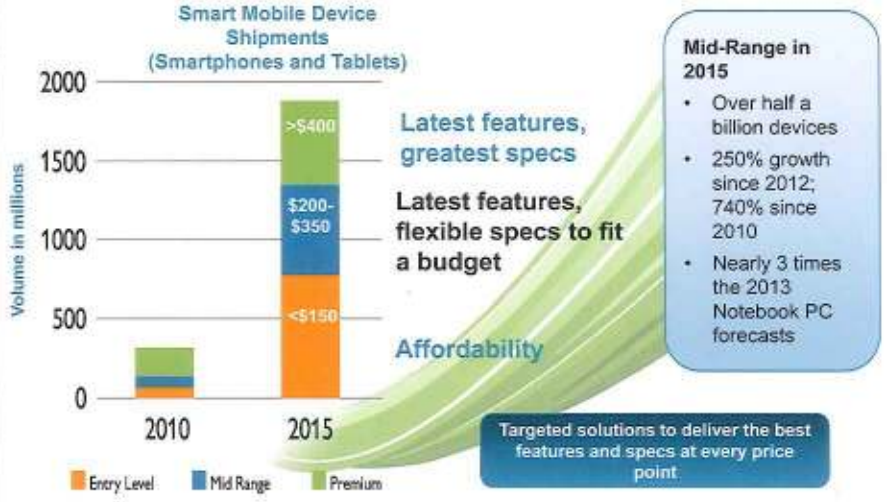
Raviraj Mahatme
Platform Marketing Manager
ARM, San Jose

Today's Mobile Computing World

- Over 1 billion smartphones to ship in 2013*
- Smartphones from <$50 to tablets >$800
- Tablets out-ship notebook PCs

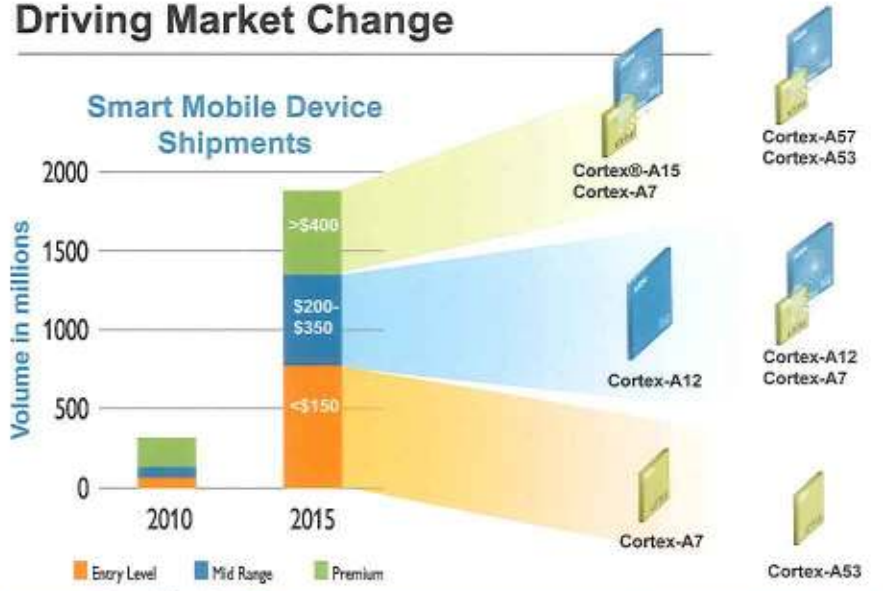
*Bank of America Merrill Lynch estimate

Growth Driving Multiple Price Bands



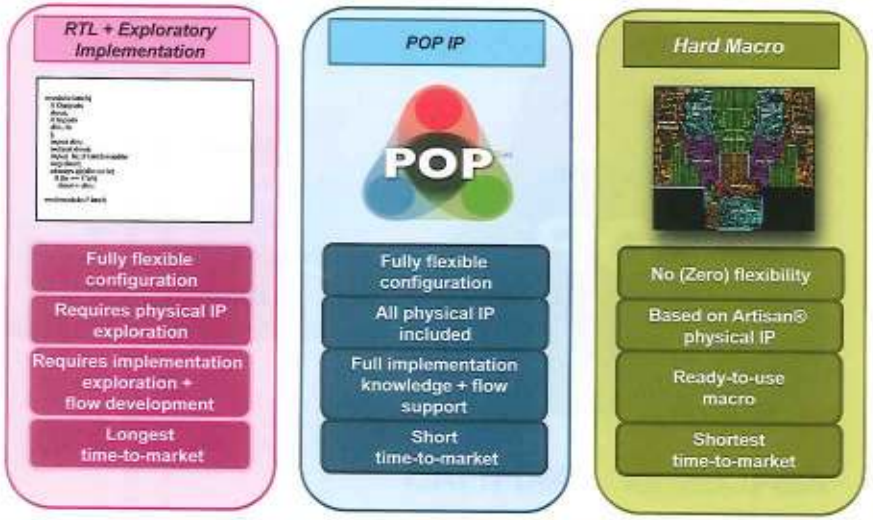
Mixture of ARM and Gartner Estimates

Driving Market Change



Mixture of ARM and Gartner Estimates

POP IP: Cortex-A Implementation Alternative

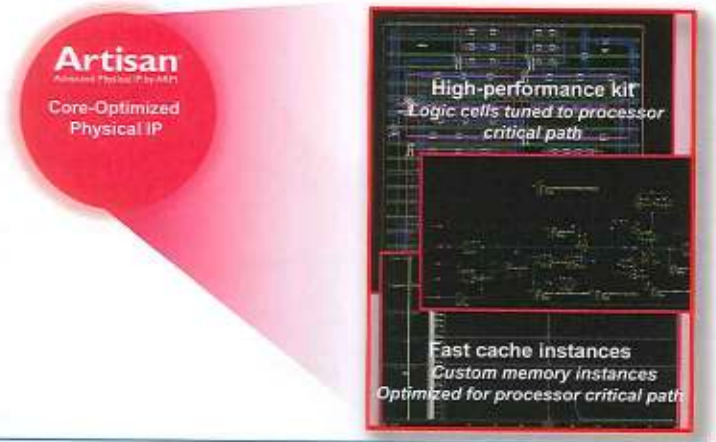


The ARM POP IP Solution

- ***Best PPA for ARM Cortex processors and Mali™ GPUs***
 - Driven by ARM low-power implementation knowledge
- ***Fastest Time-to-Market***
 - Leverages ARM implementation expertise and knowledge transfer
 - Fastest design cycle of ARMv7 32-bit and ARMv8 64-bit Cortex processors as well as Mali-T600 series GPUs
- ***Co-Developed with Processor Engineering Teams***
 - Supports the newest cores right from product introduction
 - Incorporates the latest ARM innovations
- ***Enables Tailored Implementations***
 - Multiple configurations of cores to optimize for power, performance and area

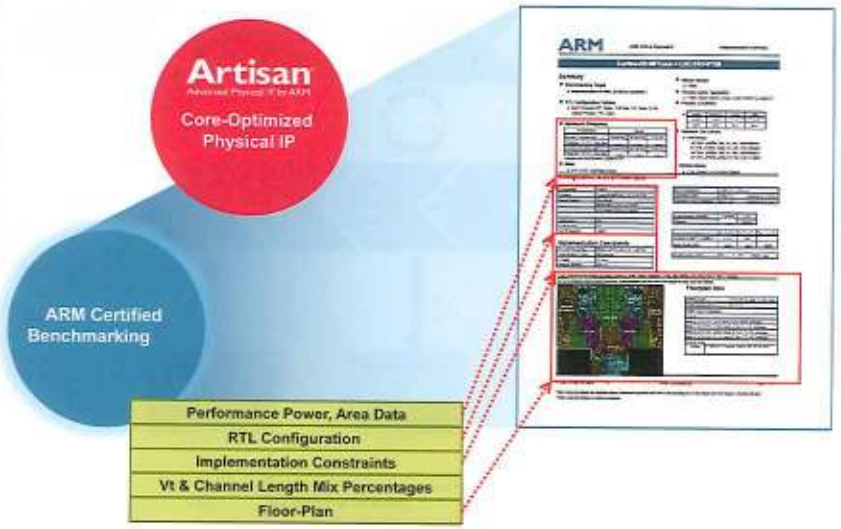


POP IP: Physical IP

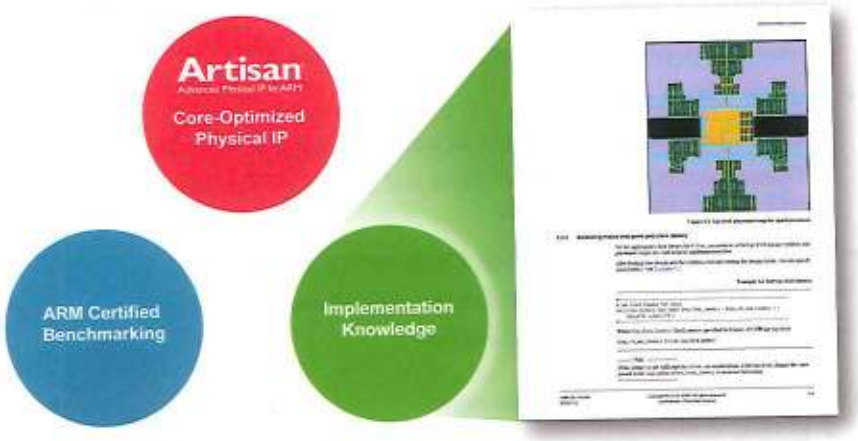


40G, 40LP, 40LP+, 28LP, 28LP+, 28HPM, 20SOC and 16FF

POP IP Benchmarking- For Detailed Proof-Point



POP IP: Unique ARM Core Expertise



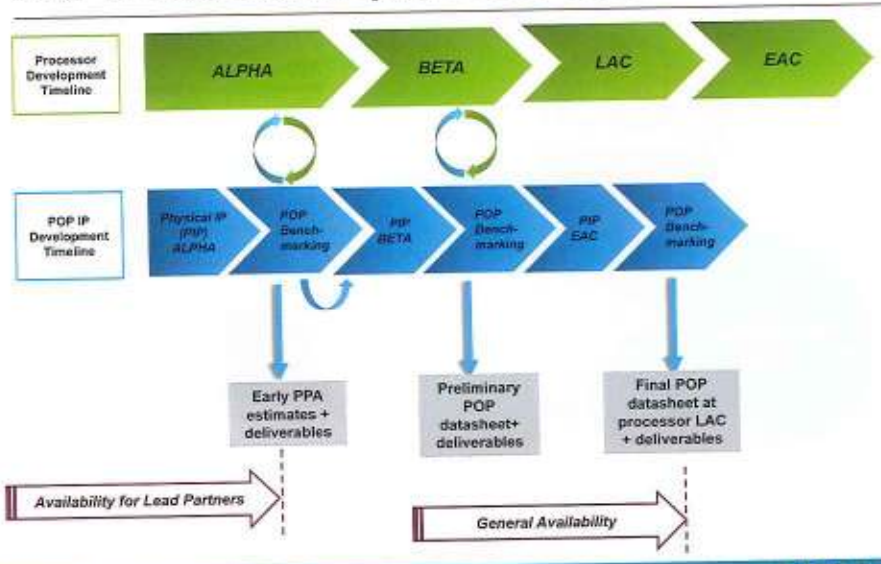
POP IP: Core-Hardening Acceleration



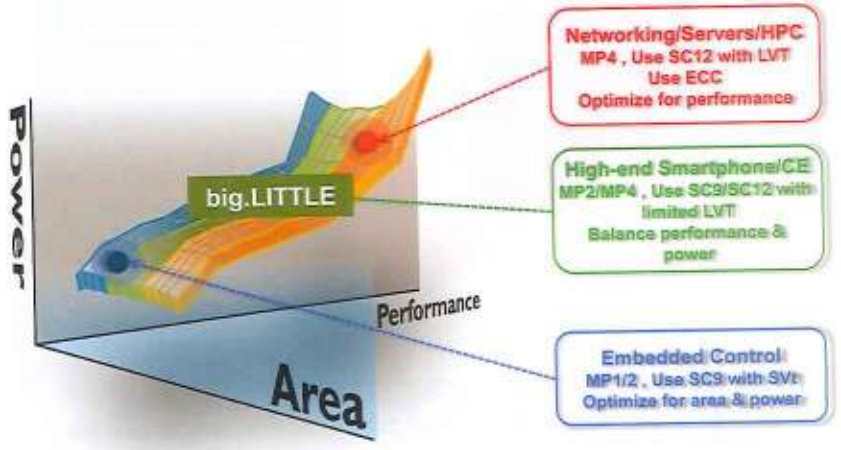
New Processes
New Cores
Improved PPA

ARM CORTEX Processor Technology
ARM MALI Graphics Technology

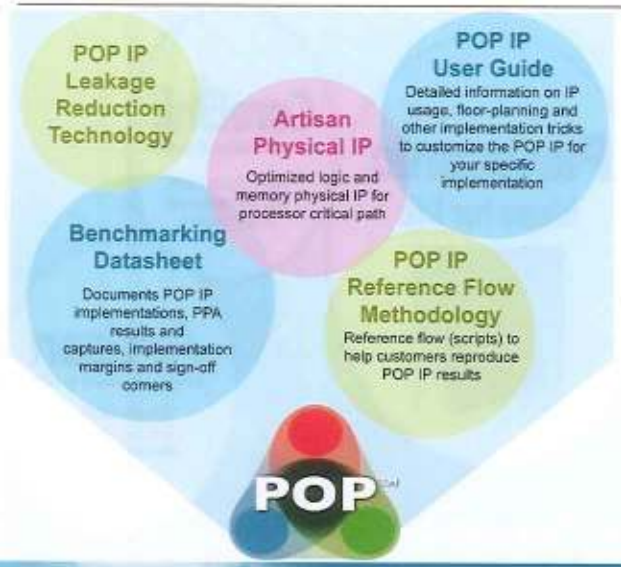
POP IP: Co-Developed & Co-Optimized



POP IP Delivers Broad PPA Envelope



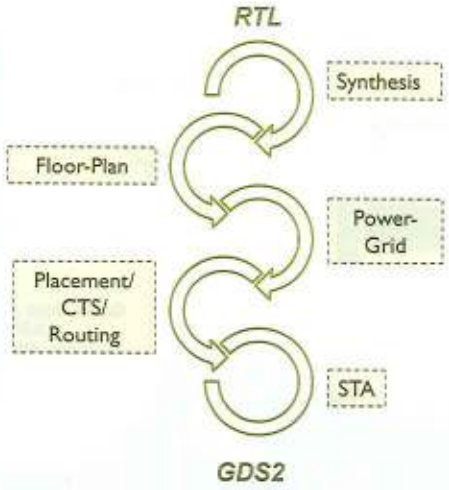
What's Included in POP IP?



POP IP Delivers Complete RTL-GDS2 Flow

POP IP Reference Flow Methodology

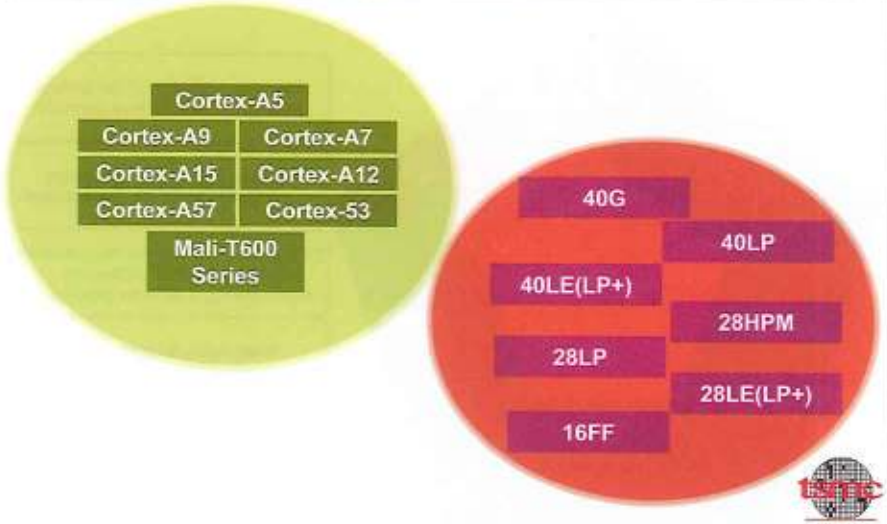
- Complete Synopsys- or Cadence-based flow (scripts)
- Reproduce POP IP benchmarking PPA



ARM POP IP Beats the Competition.....

ARM POP IP	Competing Solutions
POP IP can provide a range of reproducible PPA data-points **before** start of implementation	Cannot provide proof of PPA before start of implementation
Complete integrated solution from one company	Competitors can only provide piece-meal solutions & the customer has to deal with different companies for support
Access to ARM low-power implementation knowledge	ARM does not support third-party physical IP for implementation solutions
Developed in synergy with Cortex-A or Mali architecture teams	Competition has no access to ARM Cortex-A or Mali RTL

ARM POP IP on TSMC Process Technologies



Onda™ V818 Mini



ONDA

Artisan
Advanced Physical IP by ARM

Cortex
Low-Power Leadership from ARM

全志科技 Allwinner Technology

Quad-core Allwinner® A31s
Quad-core ARM Cortex -A7 processor-based SoC
ARM 40LP POP IP for TSMC
40nm LP technology
ARM DS-5™ Toolchain

ARM processor-based devices powered by Android™ 4.1 Jelly Bean

ARM Connect. Collaborate. Create.

Panasonic Smart TV Chip

Cortex
Low-Power Leadership from ARM
1.4 GHz dual core ARM Cortex-A9 MPCore processors

Panasonic
ideas for life



CoreLink
Intelligent System IP by ARM
ARM CoreLink™ NIC-301 Network Interconnect

Artisan
Advanced Physical IP by ARM
ARM POP IP for Cortex-A9 on TSMC 40nm LP process technology

ARM Connect. Collaborate. Create.

The Architecture for the Digital World® ARM

POP IP: Best Implementation Solution for ARM SoC



- Available at POP LAC for fastest time-to-market for lead partners
- Co-developed with processor to achieve synergistic optimization
- PPA on POP IP is highly reproducible leveraging POP reference methodology & Artisan physical IP
- Thoroughly benchmarked; All physical IP is silicon validated
- POP IP enables fastest time-to-market for Cortex-A licensees

The Architecture for the Digital World® ARM

Thank You

The Architecture for the Digital World® ARM

NOTE

A Highly Configurable and Robust Memory Subsystem for Multi-core SOCs in Advanced TSMC Process Nodes

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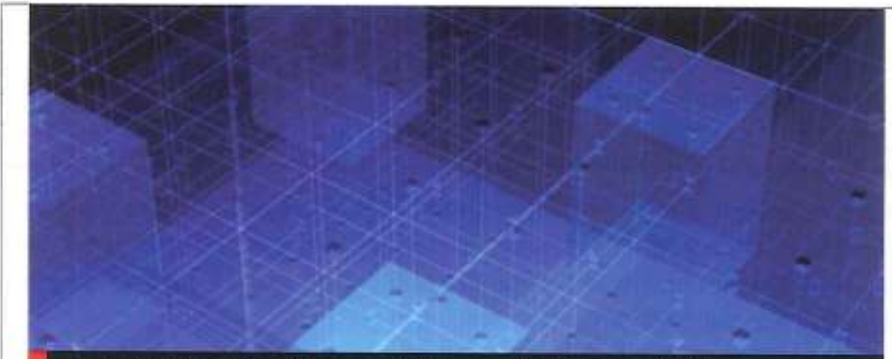


ABSTRACT

Today's multi-processor SOCs in advanced technology nodes place increased demands on memory throughput. This requires tuning the memory sub-system to the unique demands of each application ranging from high-performance enterprise supercomputers to power-efficient handheld consumer units. How do you evaluate memory subystem IP to determine if it is flexible enough to support the configuration and performance you need? Finally, how do you configure interconnect and memory subsystem to optimize your system performance?

This paper describes a new paradigm for addressing the challenges of measuring and debugging performance use cases for multi-processor SoCs in advanced technology nodes. By examining different implementation options for multicore processors and Cadence memory susbsystem IP under different use cases, users can build a clear picture of the impact of these design decisions on system performance. Trade-offs can be made to find optimum implementation options and QoS configurations for given system use cases defined by a collection of traffic profiles. A new tool, the Interconnect Workbench is introduced to demonstrate this new paradigm.

Cadence memory subsystems are optimized to reduce operating power and to minimize leakage power associated with advanced technology nodes. Design techniques to enhance yield in 28nm and lower technologies through robustness to OCV and improved ESD will be discussed.



A Highly Configurable and Robust Memory Subsystem for Multi-core SoCs in Advanced TSMC Process Nodes

Wendy Elsasser, Architect DDR IP
Gopal Raghavan, CTO, IP Group
Nick Heaton, Sr. Solution Architect
October, 2013

cadence

Outline

- Importance of memory subsystem in SoC
- Interconnect Work Bench – tool to profile subsystem performance
- Performance optimization using configurable memory controller
- Design approach to improve robustness
 - Digital v/s analog DLL
 - OCV tolerance
 - Improved ESD

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ARM® CoreLink™ 400 System IP

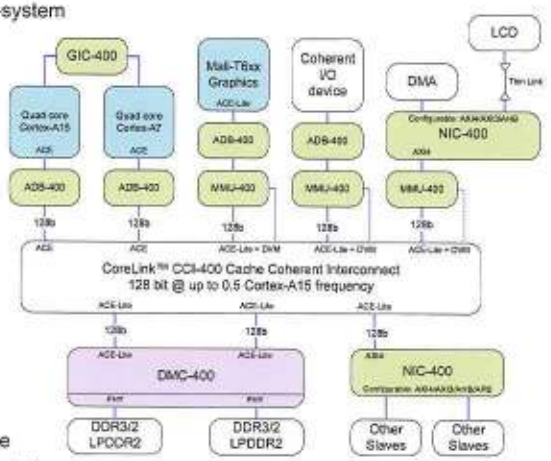
IP you need for your compute sub-system

- Processors
 - Cortex®-A15
 - Cortex-A7
 - Mali™-T6xx



CoreLink Intelligent System IP by ARM

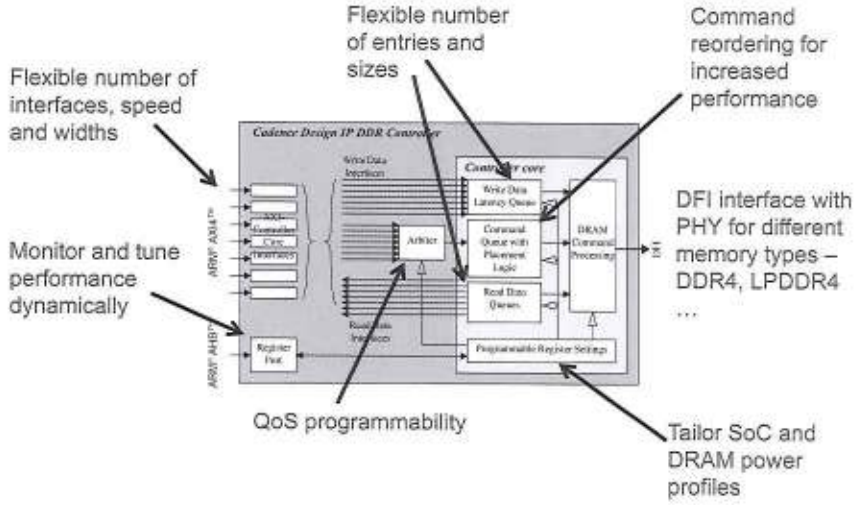
- GIC-400 Generic Interrupt Controller
- MMU-400 System Memory Management Unit
- CCI-400 Cache Coherent Interconnect
- NIC-400 Network Interconnect
- ADB-400 AMBA® Domain Bridge
- DMC-400 Dynamic Memory Controller



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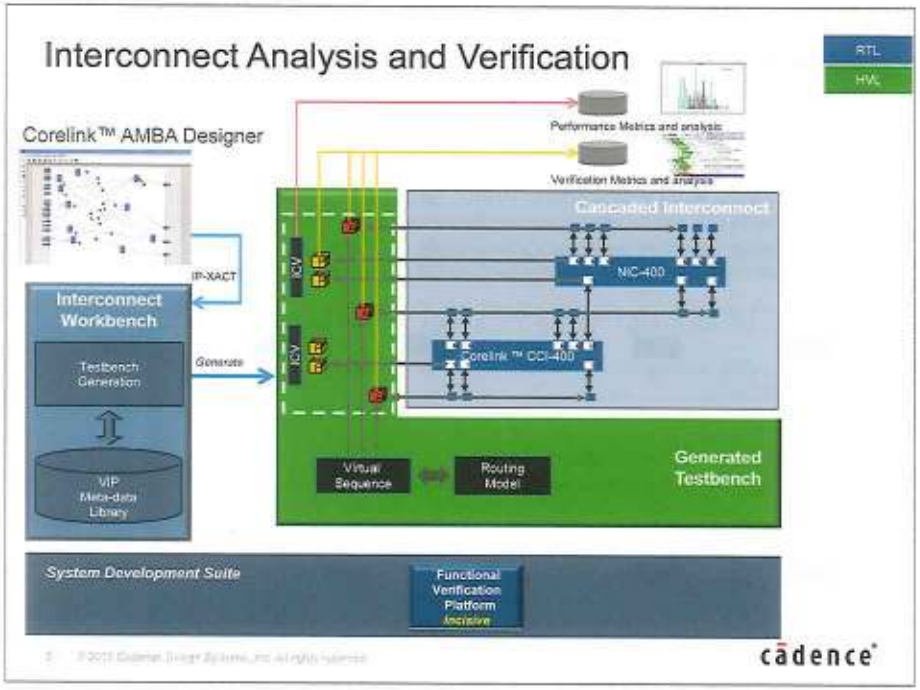
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Cadence Configurable Memory Controller



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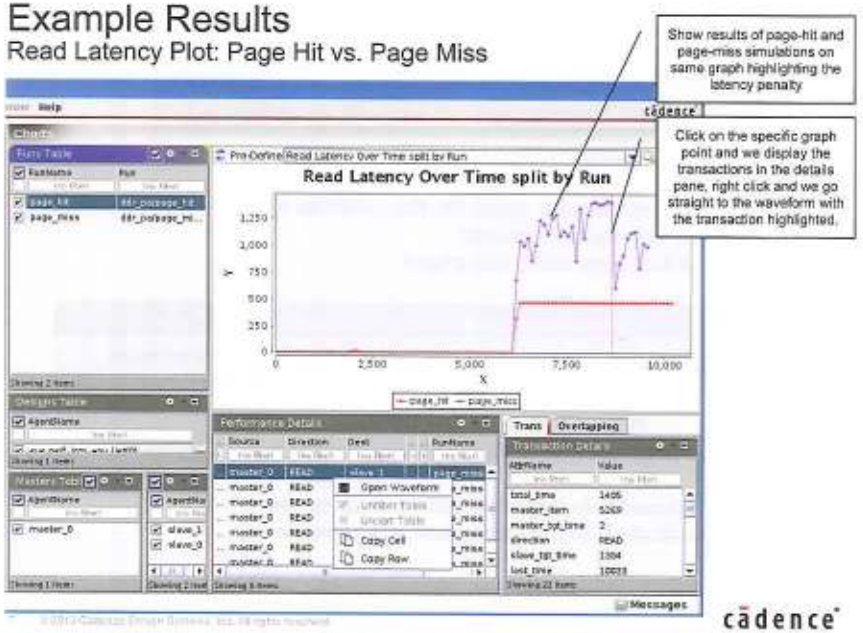
Basic Performance Sequence/Scenarios

- Available Sequences
 - Sanity test – One write and one read
 - W-W-W-W-W (back to back writes)
 - R-R-R-R-R-R (back to back reads)
 - WWWWW-RRRRR-WWWWW-RRRRR (Bursty traffic)
 - W-R-W-R-W-R (Turnaround testing)
 - Page hit test sequence (Write/Read sent to same page address)
 - Page miss test sequence (Write/Read sent to different page address)
 - Bank cycling test (Continuous commands sent to different banks in a cyclic manner)

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Example Results

Read Latency Plot: Page Hit vs. Page Miss



DDR3 Performance Optimization

Configuration Details

- 2 Ports – Dedicated WR and RD ports
- Mem. Data Width – 32 bits
- Address Width – 32
- No. of Chip selects – 1 (to force more bank collisions)
- No. of Queues – 3 (Write, Read and Command)
- Queue Depth – Write (64), Read (32), Command (32)
- Address Input (device, row, bank)
- Clock Frequency – 933 MHz
- Equal command arbitration across ports
 - Neither port starved out

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DDR3 Performance Optimization
Programmable Features Tested

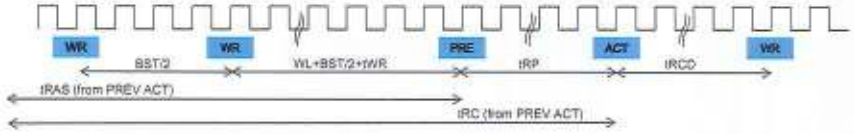
- Out of Order Processing
 - Case 1: Disable re-order capability of write commands from the same source ID
 - Case2:Enable re-order capability of write commands from the same source ID
- Address Coherency Granularity
 - Case 1: Page granularity
 - Case 2: Sub-page granularity; dynamic granularity based on command length

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Targeted Performance Sequence
Sequence 1 – Write Command Re-order Test

- Commands aligned to burst boundary
- Command length 2 DRAM burst
- Continuous write commands (Port0) and read commands (Port1)
 - Packets of 4 back-to-back commands per port access same bank, different row
- Simulated with following programmable options:
 - Write command re-ordering disabled; worst case timing illustrated below



 - Write command re-ordering enabled
 - Number of B2B writes dependent on re-order depth

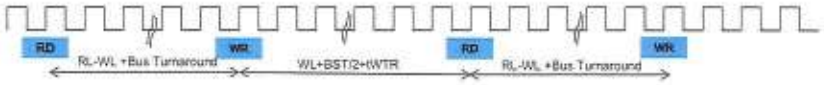


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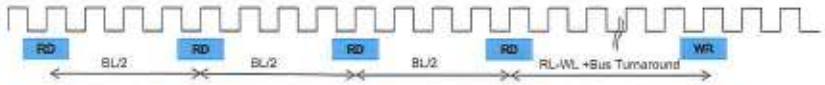
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Targeted Performance Sequence
Sequence 2 – Address Granularity Test

- Commands aligned to burst boundary
- Commands 1 burst in length
- Alternating read and write commands
 - All commands are to the same bank
 - Row address increments every 4th write command; Random, non-overlapping column addresses
- Simulated with following programmable options:
 - Page granularity address collision check
 - Cannot group commands to the same page due to address collision with WR CMDS



 - Sub-page granularity address collision check
 - Dynamic address collision check based on command size
 - No address collisions detected; controller has full re-order capability



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DDR3 Performance Results

Utilization Improvement (Sequence 1)	
Without WR CMD Reorder	With WR CMD Reorder
60%	100%

With increased re-order capability, the controller was able to:
-Optimally schedule commands
-Minimize bus open/close sequences

Utilization Improvement (Sequence 2)	
Page address collision granularity	Sub-page address collision granularity
80%	100%

With sub-page address collision checks, controller was able to group:
-Write commands to the same bank and same row
-Read commands to the same bank and same row

NOTE: Results were normalized to show peak performance (100%) with performance features enabled.

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Advantage of Digital DLL from Analog DLL

#	items	Digital DLL TSMC 28HPM Process	Analog DLL
1	Area	1x	4x (Charge Pump Cap, VCO)
2	Power	1x	2x (Charge Pump)
3	Noise tolerance	Good for both Vdd / Gnd	Weak – Vdd only
4	granularity	Fine (~9ps)	Very Fine(~6ps)

- Challenges in analog DLL in 28HPM
 - Mismatch effects on step linearity
 - In IP case, minimum metal stack usage results in larger area

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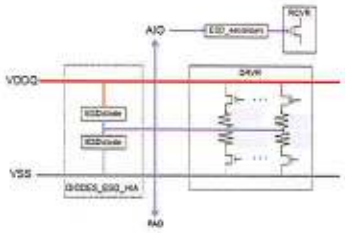
Architectural Solutions for OCV in TSMC 28HPM

- Reduce clock duty cycle distortion
 - Single edge dependence
- Clean up external clock DCD
 - Internally re-generated clocks
- Internal PLL
 - Isolates against OCV outside of PHY
 - Protects against external CLK-to-CLK OCV
- Locally grouped delay lines

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Robust ESD Design of DDR I/O in TSMC 28HPM

- Common Vss used with multiple Vdd's domains required by DDRx specification and to improve noise immunity.
- Low capacitance and high ESD tolerance
 - Custom layout for high speed I-Os to increase ESD levels and reduce parasitic capacitance.
 - Low capacitance is a key performance driver
- Maintain low resistance from pad to clamps and I-O diodes to clamps through automated EDA tools that checks for bottlenecks and current density.
- Careful layout of core transistor drivers and secondary protection structures to boost robustness.





ESD Diode in 28HPM

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Configurable, Robust Design for Advanced TSMC Process Nodes

- Multi-processor SoC's require advanced technology nodes and increased memory throughput demands
- Multiple use cases with different system requirements
- Configurable Cadence Controller+PHY solution allows optimizations for a variety of systems
 - Work Bench profiles subsystem performance
- Design techniques improve yield, robustness to OCD, improved ESD, etc.

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Design Optimization Kits: Complete Physical IP Solution for Optimizing CPU and GPU Core Implementations in TSMC 28HPM Process

Imagination Technologies & Synopsys

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

The implementation of all the processors on an SoC has a significant impact on the overall performance, power and area ("PPA") of the chip. But there is no one-size-fits-all design point for CPU, GPU and DSP processors; design teams are driven by the competitive requirements of their end applications and must optimize each for speed, power, or area -- or optimal balance of all three. Utilizing design flows tuned for specific processor cores, pre-optimized floorplans and enhanced embedded memories and logic libraries can yield significant improvements in processor PPA and significantly reduce the time spent optimizing the implementation to meet PPA targets. In this presentation, Imagination and Synopsys will present the latest results achieved from their collaboration on Imagination's PowerVR Series6 GPU and MIPS CPU cores implemented in TSMC's 28HPM process. The session will cover the unique needs of CPU and GPU optimzations and how using Synopsys' optimized high-speed and ultra high-density memories, high-speed flip-flops, multi-bit flip-flops and datapath cells helped improve the performance, power and area of Imagination's GPU and CPU cores. In addition, the session will describe how processor-tuned design flow scripts enabled the team to achieve the PPA improvements with a 30% faster implementation turnaround time.

The resulting Design Optimization Kits (DOKs) for Imagination's processor cores will enable designers to accelerate design closure at their target PPA specifications and speed time-to-market.

Imagination

Design Optimization Kits: Complete Physical IP Solution for Optimizing CPU and GPU Core Implementations in the TSMC 28HPM Process

Vikas Sethi (Synopsys) and John Herbert (Imagination)

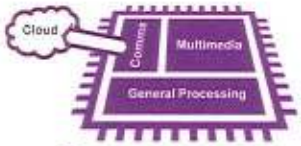
www.imgtec.com

Agenda

- Introduction to Imagination
- Challenges of GPU and CPU implementations
- Introduction to Design Optimization Kits (DOKs)
- Physical IP for processors – HPC Design Kit
- PowerVR G6100 DOK results
- Summary

Imagination Technologies Overview

- **Leading silicon, software & cloud IP supplier**
 - Multimedia, processors, communications, cloud
 - Licensing & royalties based business model
- **Targeting high volume, high growth markets**
 - Semiconductor manufacturers and OEMs
 - Mobile, home consumer, automotive, storage, networking, infrastructure, IoT
- **Pure: our strategic product division**
 - Digital radio, connected audio, home automation
- **Established technology powerhouse**
 - Founded 1985; London FTSE 250 (IMG.L)
 - UK HQ; global operations with ~1,500 employees



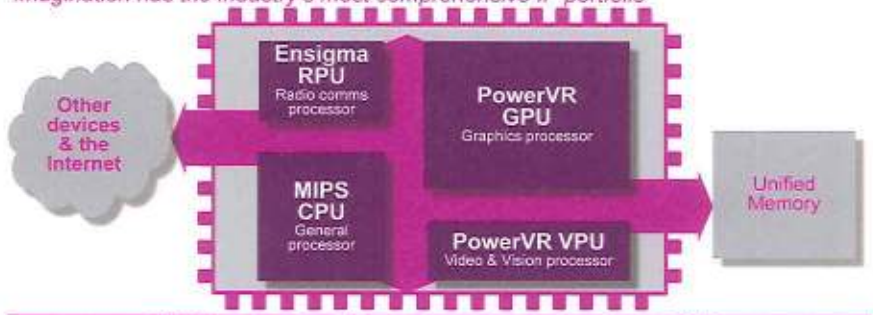
Imagination *Comprehensive IP portfolio for SoCs & cloud connectivity*



PURE *IP business pathfinder Market maker/driver*

SoC IP for Every Market

Imagination has the industry's most comprehensive IP portfolio



All of Imagination's IP stand as class leaders in their field, and also work together to create unrivalled solutions for our increasingly connected, media-rich world

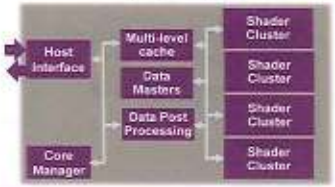
GPU Graphics: Beauty and Brains Together

- **Graphics defines the user experience**
 - Apps use graphics to make complex tasks easy and fun
- **GPU compute: The future of high performance processors**
 - Most silicon-efficient programmable processors available
 - 10x-100x the horsepower of the CPU on the same SoC
 - Performance scales linearly with area, unlike CPUs



PowerVR Series6 'Rogue' GPU

- Leading GPU for mobile applications (source: JPR)
- Leadership in performance per mW, bandwidth, latency
- Same GPU for graphics and compute - no compromises
- 100+ GFLOPs already shipping; up to 1TFLOP coming
- Ray tracing capabilities coming soon



GPUs are driving the future of SoCs and silicon processes

Imagination

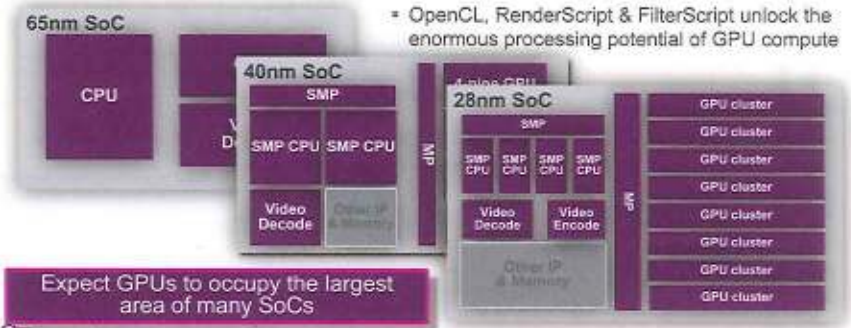
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GPUs: Increasingly Dominating SoC Processing

GPUs: data parallel architectures

- Touchscreen displays and graphics powering latest user interfaces and applications
- GPUs are inherently more scalable than CPUs
- OpenCL, RenderScript & FilterScript unlock the enormous processing potential of GPU compute



Expect GPUs to occupy the largest area of many SoCs

Imagination

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Physical Design Optimization

SYNOPSYS + Imagination

Tuned Synopsys IP and reference design flows for optimized implementation



High-performance, ultra-low power GPU

Performance-tuned libraries and memories



Automated, Galaxy-based production flow and implementation expertise



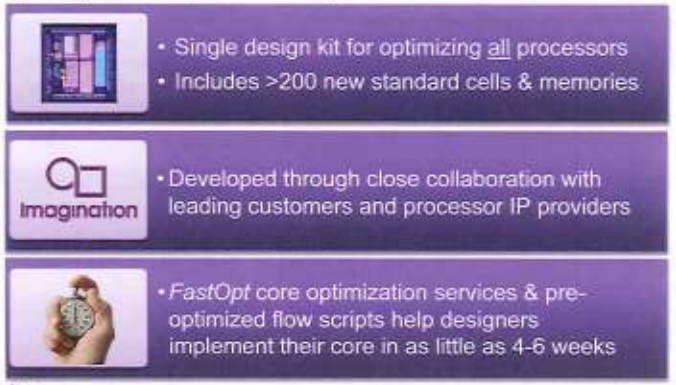
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Synopsys DesignWare HPC Design Kit

Yields superior processor performance, power & area

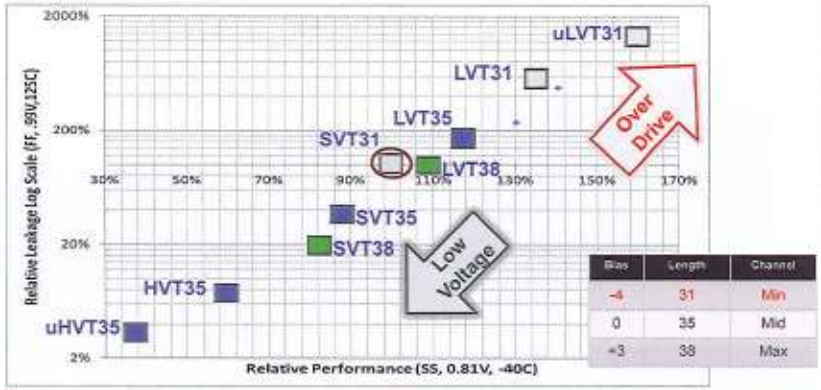


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28HPM Multiple VTs and Gate Lengths



Bias	Length	Channel
-4	31	Min
0	35	Mid
+3	38	Max

DesignWare HPC Design Kit Component Summary

Components for all types of processors

- For GPUs, emphasis more on area and power
 - Mbit registers and UHD/HD memories are a must
- For CPUs, frequency is the main driver
 - High speed flops and SD memories are key
- DSP
 - All of the above

Component	CPU	GPU	DSP	Primary Benefit
Logic Library				
High-Speed Flops	●		●	Critical path performance
Area-optimized Flops		●	●	Register area
Multi-bit Flops		● ●	● ●	Dynamic power/Area savings
Delay Cells	● ●	● ●	● ●	More accurate hold fixing
High-Density MUXes		●	●	Minimize routing congestion
Memory				
Fast Cache Instances	●		●	Critical path performance
Ultra High-Density 2 Port Compiler		● ●		Reduces area and leakage
High-Density Single Port Instances			● ●	Reduces area and power

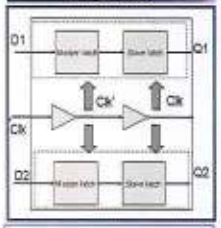
NOTE: Pre-optimized flow scripts and core optimization services also available

Optimized for: ● Performance ● Power ● Area

IP That Makes a Difference in GPUs

DesignWare standard cell embedded memories

Multi-bit Flip-flops



- Reduce clock tree loading
- Reduce area and leakage

Ultra High Density Two Port Register Files

28nm	HD 2P RF	UHD 2P RF
Area	1	0.52
Bit Density (Mb/mm²)	1	1.91
Access Time	1	0.90
Cycle Time	1	1.55
Leakage	1	0.67

48% lower area

33% lower leakage

- Reduce leakage
- Reduce area

- Benefits confirmed by DOK

Area benefits of DesignWare HPC Kit

	Base	HPC Kit	Saving
DCG	4.844	4.562	6%
Place Opt	4.855	4.574	6%
Route Opt	5.432	4.974	8%

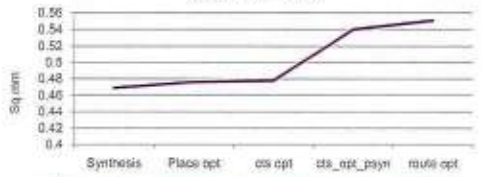
Power benefits

Block	Leakage	Dynamic
A	0%	21%
B	29%	27%
C	24%	23%
D	13%	27%
Total	20%	25%

DesignWare HPC Design Kit

Benefit of multi-bit flops

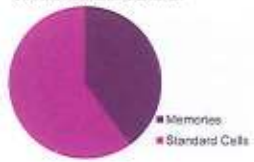
Area increase using 13% OCV and 60ps hold margins (Typical 28nm result)



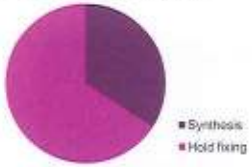
Hold fixing comparison - MCMM single bit registers (in sq mm)

	Single-Bit	Multi-Bit
30ps	0.478	
40ps	0.491	2.808
50ps	0.511	6.852
60ps	0.540	12.971

Cell area savings (Synth)



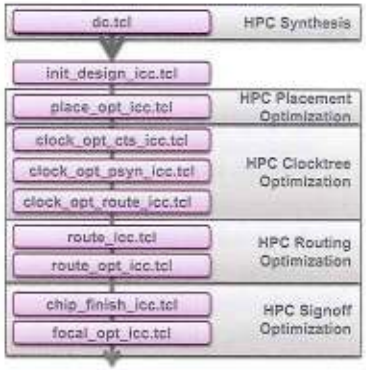
Multi-bit flop area savings (Final)



Synopsys High Performance Core (HPC) Flow

Great results first-time

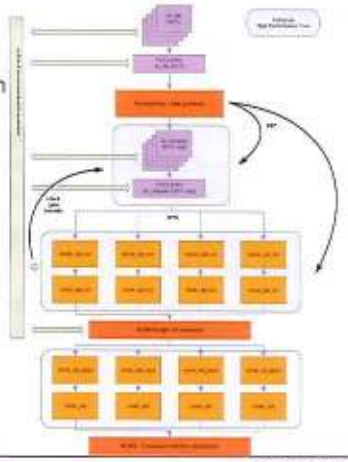
- DC Graphical (DC-G) optimized flow with Synopsys Physical Guidance (SPG)
 - Run physically-aware synthesis with SPG
 - Same physical constraints as place & route
- IC Compiler (ICC) SPG placement based on DCG result
 - Perform critical optimization & Congestion removal
- ICC Clock-Tree Synthesis (CTS)/ Clock-Tree Optimization (CTO)
- ICC optimized routing
- ICC signoff



Building on HPC

DOK reference flow a superset of HPC

- Currently HPC emphasis is block level, but high performance cores are hierarchical
 - Supplementary flow scripts created to address this limitation
 - Available as standalone DCG/ICC scripts from Imagination or via a Lynx plugin supported by Synopsys Professional Services
- Includes
 - Updated DCG scripts to support register retiming
 - Inclusion of budgeting to enable near-abutted floor plans
 - Top-level P&R and integration scripts



Register Retiming

Building on HPC

- As part of DOK creation we need a means to reliably achieve optimal register retiming results
 - Currently solution based upon trial and error approach and is not floorplan aware.
 - Adopted a characterization approach

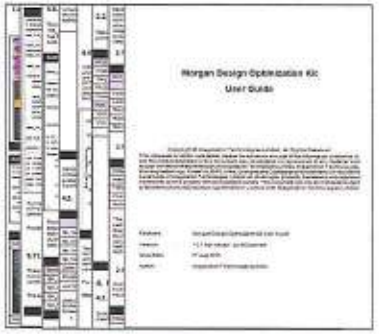
- 25% reduction in area
- 10% reduction in Flops

Improvement

	Timing		Area		Flop Count	
Block	HPC	Default	HPC	Default	HPC	Default
A	0.02	1.68	1631	1655	194	264
B	1.23	1.78	1017	670	108	122
C	1.07	1.41	762	924	70	73
D	1.88	1.5	697	960	128	91
E	1.38	1.71	526	646	61	62
F	1.69	1.34	1497	3182	83	229
G	1.86	2.04	1806	2887	162	109
H	1.87	1.5	800	1181	91	74
TOTAL			8837	12105	897	1024

PowerVR G6100 DOKs Available Now

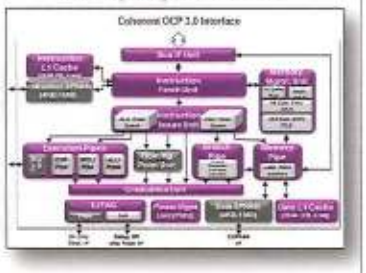
- All objectives met
 - Achieved targeted performance goals
 - 10% area savings achieved at the targeted frequency
 - Up to 25% reduction in power
 - Hierarchical reference flows available
 - Available in standalone HPC flows from Imagination
 - Lynx plugin available from Synopsys
 - Reference floor plans available
 - Achieve area guidance for metal stack options
 - Documentation available
 - Complete 50-page implementation guide to assist physical integration



MIPS proAptiv CPU Optimization

- proAptiv: superscalar, multi-issue, out-of-order
 - Designed for the latest application software
 - Optimized for peak single thread performance
 - Pure RISC ISA - ideal for dynamic compilation
- Taking work we've done with GPUs; applying to CPUs
 - Dual-core proAptiv CPU cluster with Coherency Module (CM2) including L2 cache

MIPS proAptiv CPU core



Summary

Imagination and Synopsys' successful partnership

- Provides the very best solution for customers
 - Combines proven IP with scalable, predictable flows and services for IMG cores
 - Leveraging individual expertise to deliver combined, optimized solution that significantly improves PPA
- Customers to meet their goals
 - Accelerates time-to-market
 - Enables improvements in quality of results
- Collaboration effort already yielding improved results
 - Expecting greater improvements with aggressive area/power improvements



SYNOPSYS® Imagination

NOTE

An Antifuse-based Non-Volatile Memory for Advanced Process Nodes and FinFET Technologies

Sidense

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

Non-volatile memory (NVM) is a vital component for most ICs used across the electronics industry including those used in mobile, computing, and automotive applications along with the growing range of devices that will comprise the evolving "Internet of Things" (IoT). Antifuse-based one-time-programmable (OTP) memory, in particular, meets many NVM requirements as a replacement for ROM and eFuses, providing code and key storage and for trimming and device configuration.

Sidense's antifuse-based single-transistor OTP (1T-OTP) is already proven in a range of TSMC process technologies, having passed IP9000 Assessment in partnership with TSMC for many, and 1T-OTP macros are embedded by many leading semiconductor manufacturers in their devices. The scalability and portability across process nodes and variants also makes 1T-OTP a compelling NVM choice for devices fabricated in advanced technologies.

This presentation will discuss Sidense's 1T-OTP technology, its applications and how it fits the requirements for devices manufactured in advanced process nodes. Already proven in HKMG technology, the excellent results of 1T-OTP in these processes will be shown. Sidense will also present the 1T-OTP roadmap moving beyond 20nm into FinFET processes and the expected benefits that Sidense's 1T-OTP architecture will bring to TSMC customers.

Sidense

The Future of Logic NVM™

An Antifuse-based Non-Volatile Memory for Advanced Process Nodes and FinFET Technologies

Betina Hold – Director of R&D, Sidense

TSMC Open Innovation Platform
October 1, 2013

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Agenda

- OTP Markets and Applications
- NVM and the Importance of OTP
- 1T-OTP Overview, Products
- SHF for Advanced Process Nodes
- SHF Application Implementations
- Collaborations with TSMC
- Advanced Process Nodes

Target Markets and Applications



Mobile Handset | Notebook PC | Automotive Industrial | Digital TV | Games PMPs | IoT | Communications

Need for OTP in ICs

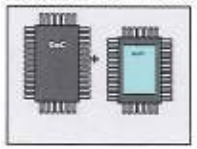
Processor Configuration | Image Sensing | Power Management | Analog, Audio, RF | Display, Touch Screen | Sensors, Connectivity, Timing...

OTP meets the need for:

- Secure Code Storage
- Secure Key Storage
- Analog Trim
- Calibration
- Device Configuration
- Device ID

Non-Volatile Memory

Discrete NVM Devices



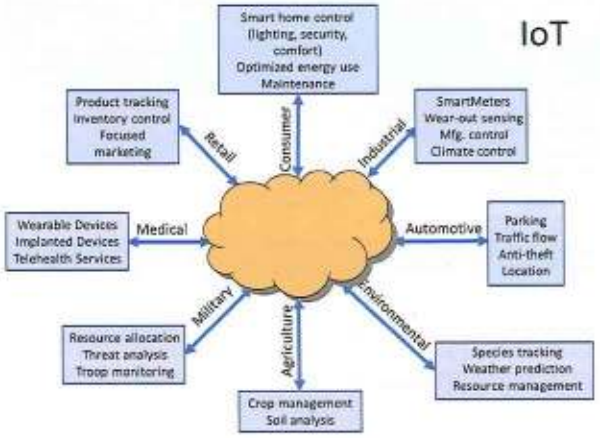
	Technology
Flash	Floating gate. Block erase
EEPROM/PROM	Floating gate.
MRAM	Magnetic storage
RRAM	Resistance change
PCMRAM	Resistance change/phase change

NVM embedded on chip



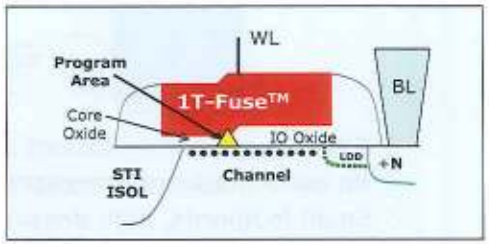
	Technology
Antifuse OTP	Permanent and controlled oxide breakdown, on-chip programming
Fuse/eFuse	Polyfuse/ metal fuse blowing
Mask ROM	ROM pattern fabricated on-chip
Flash/MTP	Floating gate. On-chip erase/program
MRAM, RRAM, PCMRAM	Emerging memories

IoT Ecosystem: Vast NVM Opportunities



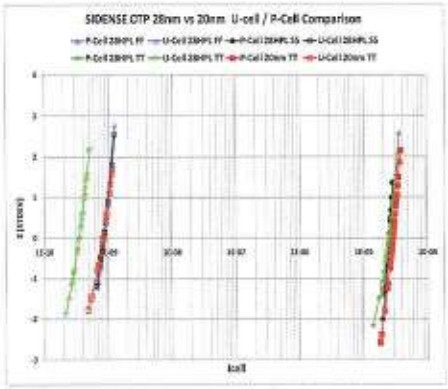
Antifuse-based Sidense 1T-OTP Bit Cell (1T-Fuse™)





- Patented 1T Split-Channel OTP architecture
- Reliably programmed through a controlled DBIE
 - **Dielectric Breakdown Induced Epitaxy**
- Non-reversible **Nano-crystal** formed between channel and gate
- Programming from charge pump or VPP pin

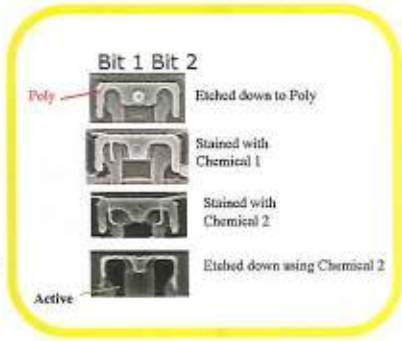
1T-OTP: Reliable & Programmable



- 28nm to 20nm
- Excellent Cell Margin
 - Across process nodes
 - Across process splits
 - No leakage
 - No tail

Highly Secure NVM for Key, Code and Data Storage

- 1T-OTP Bit Cell:
 - Very difficult to reverse engineer
 - No charge stored in the bit cell
 - No visible difference between a programmed and an un-programmed state
- 1T-OTP Macro:
 - No Read Power signature
 - Secure OTP Boot procedure
 - Program lock
 - Differential/Multi-cell read mode for additional power supply Margin
 - Metal Shielding



Sidense 1T-OTP Macros

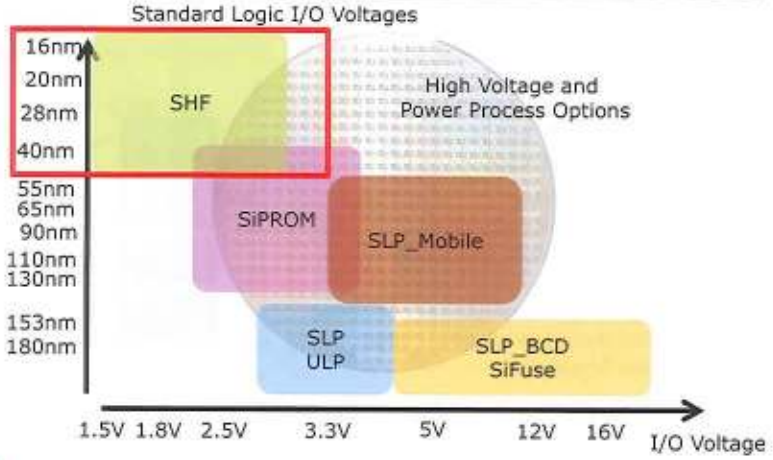


- *Silicon proven from 180nm to 20nm with TSMC*
- No extra masks or processing steps
- Small footprints, high densities:
 - Minimal impact on die area and cost
 - Power-efficient
- Very secure and reliable
- Read mode options support lower voltage operation
- Field programmability
- Easy conversion to ROM

1T-OTP Product Comparison

Product Family	Usage (eMTP=emulated MTP)	Features	Process (Std. Logic CMOS)	Voltage (Core / IO)	Density (per Macro)	Read Modes S=Single D=Differential R=Redundant Q=Double Red DR=Diff-Red
SiPROM	ROM replacement, code, data, key storage, eMTP	High Density Fast Read Access Redundancy	130nm – 55nm	0.9 - 1.5V / 2.5V - 3.3V	8 Kbits – 512 Kbits	S, D, R, DR
SLP	Handheld, RF-ID, key, code, data, trimming, eMTP	Very Low Power	180nm – 153nm	1.8V / 3.3V	128 bits – 256 Kbits	S, D, R, DR
SLP_B (BCD)	Power Mgmt, analog, trimming, code, data, eMTP	Low Power High Voltage	180nm BCD	1.8V / 5V	128 bits - 256 Kbits	S, D, R, DR
ULP	Trimming/calibration, RFID, power-up boot	Ultra Low Power, Low Read Voltage	180nm – 153nm	1.8V /3.3V 1.5V-only Read	16 bits – 2 Kbits	DR
SHF	ROM replacement, code, data, key storage, eMTP	Fast Read, Fast Program ECC, Redundancy	40nm, 28nm, 20nm, 16nm	0.8V-1.2V / 1.5V - 2.5V	1K bits – 1.2 Mbits	S, R, Q, (D)
SiFuse	Fuse Replacement	Small Area	180nm	1.8V / 5-12V	16 –64 bits	DR
SLP_Mobile	Mobile applications	Very Low Power	55nm – 130nm BCD	1.2V – 1.5V / 3.3V – 5V	128bits – 512Kbits	S, R, D, DR

Sidense 1T-OTP Process Coverage



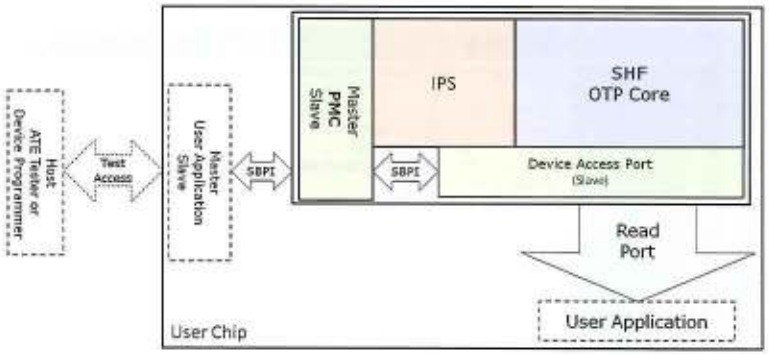
SHF: 1T-OTP for 40nm - 20nm

- TSMC Process Support
 - 40nm to 20nm
- Uses
 - Secure Code Storage, configuration, secure encryption keys, fuse replacement, ROM replacement, trimming and calibration
- Typical Applications
 - Media Processors, HDTV encryption, Network processors, Peripheral Controllers, Wireless and Interconnect
- More than OTP
 - ***System solution***

SHF Features

- High densities (up to 1.28Mbits per macro)
 - Multiple macros on a chip can provide higher capacity
- Very small footprint
- Low active and standby power
- Field programmable
- Fast read access and multiple read modes
- Integrated power supply (IPS) for in-field programming
- *Programming control and test I/F, BIST, boot control, ECC and redundancy as RTL*

SHF 1T-OTP Module



A complete solution with OTP core and IPS hard macros and RTL for interface circuitry

SHF Module Components

- OTP Core
- Charge pump (IPS) hard macro for in-field programming
 - External VPP pin for faster programming on tester
- DAP (Device Access Port)
 - provides access through SBPI and 16/32-bit parallel bus
 - SBPI provides serial and byte wide interface with SPI-compatible protocol
- PMC controls programming of data to OTP
 - PMC (Program Controller) offered in synthesizable RTL

SHF Summary

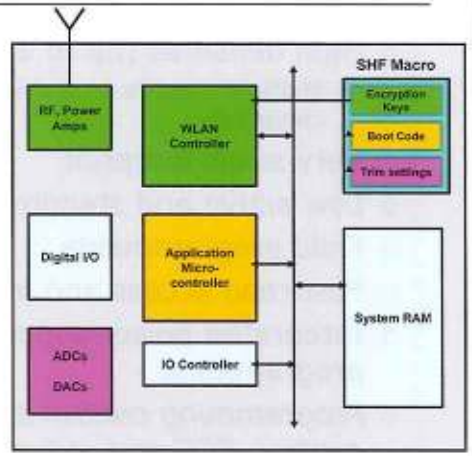
Features		Benefits
Standard Logic Processes	40nm IO voltages: 2.5V and 1.8V, 28nm, 20nm IO voltage: 1.8V	Cost-effective, highly-reliable NVM for a wide range of uses including: • Code Storage, ROM Replacement • Encryption Key, Configuration, User Settings • Fuse Replacement (Calibration, trim) No additional masks or process steps required
Small Footprints/ High Densities	Configurations from 1Kbit to 1.28Mbits/ macro with I/O widths of 8,16, 24, 32 and 40bits	
Flexible Metal Stacks	OTP and power supply use few metal layers. Top used for power supply ports and are available for routing	
Integrated OTP Module	Programming control and test interface, BIST, boot control, ECC and redundancy provided as RTL	Flexible architecture fits a wide range of system requirements
Fast Read Speed	Down to 20ns single mode (varies with configuration and process), faster redundant read modes	Execute code from OTP to reduce system cost, complexity and boot time

SHF Summary (continued)

Features		Benefits
Read Mode Options	Single, Redundant, Double Redundant	Optimize for read performance and area
Fast Program Time	For 28nm/20nm: 1µs/bit with charge pump, 5µs/word with external VPP (varies with configuration and process). OTP can be easily converted to Mask ROM	Reduce test time and manufacturing cost
Programmability	On a tester and in-field	Supports updates in-field and emulated Multi-Time Programming (eMTP)
Power Supplies	Charge pump and regulator (IPS) supplied by on-chip VCC and VDD IPS configuration options to support various system and programming requirements including regulator only (using external VPP) and charge pump options to generate programming voltages in module from VCC	Optimize for programming performance and area
Macro Compiler	Adjust macro configuration	Optimize speed/area/aspect ration
Operating Temp	-40°C to 125°C Read and Program	Data retention exceeds 10 years at full read duty cycle.

SHF Use Example – Wireless IoT Processor (TSMC40G18)

- Application Microcontroller core uses SHF macro to store boot code => activity and operation on power up
- The Wireless LAN Controller and RF circuitry (using the same SHF macro which stores boot code) uses OTP code to implement highly secure storage for encryption keys and secure communications
 - Programmed at source or in field
- Analog circuits, internal sensors, external environmental sensors, timing critical circuits, will use OTP storage for:
 - Trimming,
 - Storage of configuration settings
 - Adjustments/tuning during test and assembly as well as aging.
 - Providing in-system/in-field adjustments in final equipment



1T-OTP Customers using TSMC

- Sidense 1T-OTP macros in TSMC processes cover a wide range of application areas:

SHF applications:
- Media processors, network processors, image processors and Bluetooth

SiPROM applications:
- Media processors, HDTV, image sensors, comm., wireless proc., HDMI, mobile comm., image proc., wireless comm., medical, USB

SLP applications:
- Automotive, wireless proc., power management, touchscreen controllers, mobile comm., media proc., sensors, Bluetooth, USB

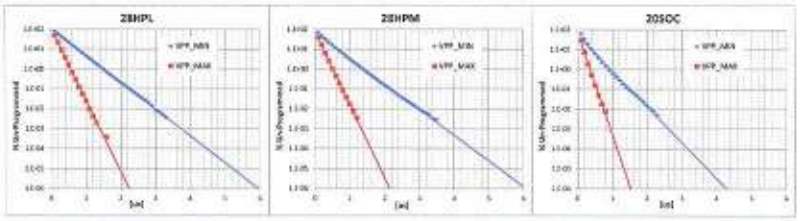
ULP applications:
- Silicon clocks, sensors

TSMC Status: 1T-OTP

Product	Nodes	Characterization Qual Report	1P9000 Complete?
SHF	40LP	●	●
	40G	●	●
	28HPM	●	○
	28HPL	●	○
	20SOC	●	○
SiPROM	130G	●	●
	110G	●	●
	110CIS	●	○
	90LP	●	●
	65LP	●	●
	65GP	●	●
SLP	180G33	●	●
	180G50	●	●
	180BCD	●	●
	152G33	●	●
ULP	180G33	●	●

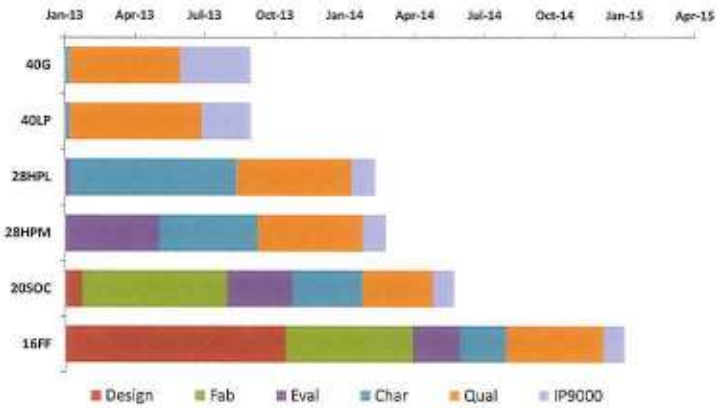
● Completed
○ In Progress

TSMC 1T-OTP: Fast and Portable



- Excellent Programmability
 - 90% of cells program in lass than a µs
 - All cells program in few µs
 - Consistent from node to node

Advanced Process Node Roadmap



1T-OTP for FinFETs

- Working with TSMC at 16nm node
- FinFET structures aligns well with Sidense OTP implementation.
- 16nm FinFET vs. 20nm 1T-OTP
 - Same bit-cell architecture and OTP design
 - Bit-cell and macro area reductions
 - Lower leakage and better performance
 - *Extra focus on circuit-level enhancements*
 - *energy efficiency and optimized timing*
 - *A complete high-level system solution*

1T-OTP for Advanced Process Nodes - Summary

- 1T-OTP SHF is an ideal OTP architecture for advanced process nodes (40nm and below)
- Proven in poly gate & HKMG gate last
- Broad TSMC process support from 40nm to 20nm with FinFET support in development.
- Sidense 1T-OTP has completed IP9000 Assessment across many nodes and process variants with more coming in 2013-2014
- Addressing critical applications such as mobile and IoT with complete system level solutions

info@sidense.com www.sidense.com

NOTE

EDA / IP / Services Track

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Power Islets: Design Methodology and Innovative Silicon IPs to Solve the Construction Quandary

Dolphin Integration

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

A major challenge of the microelectronics industry remains power management. In advanced processes, the sharp increase of leakage current becomes crucial for mobile applications, which need to combine more features, leading to exponential power dissipation with extension of usage time.

One of the most efficient solutions to reduce power may be to partition the SoC in several power and voltage islets with selective activation. The traditionnal approach to implementing such islets has some limitations in terms of islet integration and verification, relying on a mix of self-training and expensive EDA solutions.

The industry is missing some key verifications, methodology and products to fill the gaps of traditional solutions and help the SoC Integrator perform integration of islets. The Islet Construction Kit (CLICK) is THE offering to build 2nd generation power islets including attractive low power cell features with verifications, such as the methodology needed to detect and fix design issues due to high current variation (di/dt) caused by power mode transitions.

The starting point of the presentation is the description of a low-power MCU subsystem embedded in a consumer application device for which the power budget is not reached. Based on this case study, the audience will learn more about the key inputs influencing the transformation of a block into islets, and about the relevant verifications to take into consideration when implementing power islets in a design.

In the second part, an innovative methodology is introduced for limiting the impact of mode transitions on functionality, performances but also Time to Tape-out. Indeed, the impact of high current variations, inherent to islet partitioning, must be carefully checked, all along the integration flow of an islet, in order to guarantee the full functionality of the circuit and minimize the cost of late design fixes. It may take from days to weeks to assess whether a regulator can sustain the voltage drop caused both by the power mode transitions and the power-up ramps of islets. This new design methodology relies on a Mode Transition Check (MTC) to perform, at each step of the flow, a power consumption analysis, including IR Drop simulations, using a dedicated library of electrical behavioral models (EPLAM) of different elements of the power distribution network (regulator, bonding, external components, islet, power grid…).

In addition to these mandatory verifications, the intrinsic islet integration will be clearly explained in the third part. What is the best islet implementation style; how to define the optimal trade-off between interrelated parameters such as inrush current, leakage and area overhead; how to size and insert power switches and how to manage power up sequences on an islet will be some of the questions answered through the presentation. Some key cells of the CLICK offering for islet integration will be introduced together with the script for automatic sizing of power switches and their swift integration, coupled with the TRC (Transition Ramp Cell – patent pending) cell, as an alternative to complex daisy chain implementations, to manage and secure by design power-up sequences, also avoiding any iterative and complex in rush current analysis.

Power Islets

Design Methodology and innovative silicon IPs to solve the construction quandary

Gilles DEPEYROT, CTO
Dolphin Integration

Collaboration between TSMC and Dolphin

- For physical libraries: several sponsored products (memories and/or standard cell libraries) either in Nominal voltage (NV) or Dual Voltage (DV)

Technology	Std. cell	Memory					Voltage	
		SP SRAM	DP SRAM	1PRF	2PRF	ROM	NV	LV
180 eLL	✔ (6 T)	✔					1.8 V	1.2 V
180 uLL	✔ (6 T)	✔					1.8 V	1.2 V
180 uLL-HV		✔					1.8 V	
130 BCD	✔ (6 T)	✔				✔	1.5 V	
110 HV				✔			1.5 V	
90 uLL		✔		✔			1.2 V	1.0 V
90 eFlash		✔	✔	✔	✔	✔	1.2 V	
85 UP		✔					1.2 V	1.0 V
55 LP		✔					1.2 V	

- For audio codecs: collaboration for a complete offering allowing to address various applications (Smartphone, Smartwatches, Tablets, DSC, DTV, STB...)
 - 65 / 55 LP
 - 40 LP

What you will find out with this presentation: The CLICK solution

- A new **kit of cells** for power islet
 - Not only level shifters, power switches,...required for power islet construction,
 - But also
 - Ultra high density **retention cells** to reach the smallest islet area
 - **Transition Ramp Cell** to implement safely the power up sequence
 - **Scripts** to ensure a smooth integration of power islets, handling the additional tasks required in a traditional flow, with no obligation for complex User Manual
- A new **methodology** based on fast and early simulations for
 - Properly sizing the power management network (PMNet) including power regulators, external and internal capacitors to sustain the voltage drops caused by mode transitions of an islet,
 - Verifying and optimizing the power up sequence of an islet

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Content

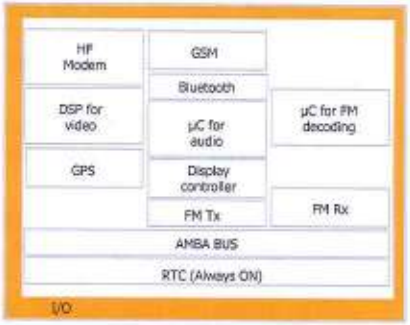
1. Introduction of SoC partitioning into power islets
2. Impact of voltage drops due to mode transitions on functionality of a SoC
3. Innovative cells and methodology to solve the construction quandary
4. Summary

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Application case description
Baseband portable radio equipment in TSMC 55 nm LP

- Various functions requiring different domains of frequency and performances
- Main constraints
 - Autonomy
 - High power consumption during short duration



Leakage represents 46% of the total power consumption of the circuit

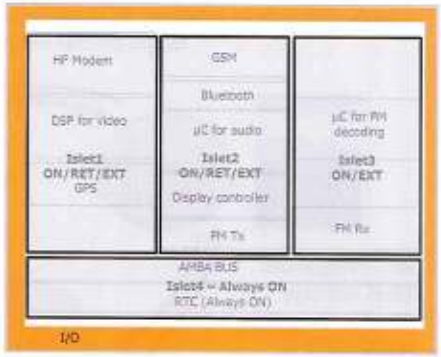
✓Leakage value is 7.56 mWh without islets, only with clock gating
✓Total power consumption value is 16.3 mWh

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Focus on islet partitioning

- Key criteria for islet partitioning
 - Activity of different blocks of the system
 - Targeted power consumption at system level
 - Voltage domains
 - Clock domains
 - Trade-off with silicon area



RET = retention
EXT = extinction

Power savings with islet partitioning

✓With islet partitioning, leakage now only represents 14% of total power consumption
✓Total power consumption is divided by nearly 2: Battery life time is significantly improved!

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Retention strategies
Live memory approach is not considered (software change required)

- The selection of the appropriate retention strategy for an islet depends on system's constraint **on wake up time**

	Retention Flop	Retention RAM	Retention Flop	Retention RAM	Retention Flop	Retention RAM
# registers	1 024 (~20 kgates)		8 192 (~160 kgates)		32 768 (~640 kgates)	
Area (um2)	6 660	8 497	53 250	58 620	213 000	227 400
Dyn. Power (uA/MHz)	0.6	2	4.9	5.2	19.7	9.6
Leakage (uW)	0.10	0.01	0.8	0.11	3.3	0.46
Wake-up time (us)	0.01	3.4	0.06	27	0.15	108

- In this presentation, retention registers is preferred due to constraints on timings

Conditions
- Comparison between Dolphin's scan retention spinner ick_rsspcnd2 and SpRAM RHEA
- TSMC 55 nm LP
- For wake up time: retention RAM @ 300 MHz ; wake up current = 10 mA

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Challenges of power islet integration for leakage reduction

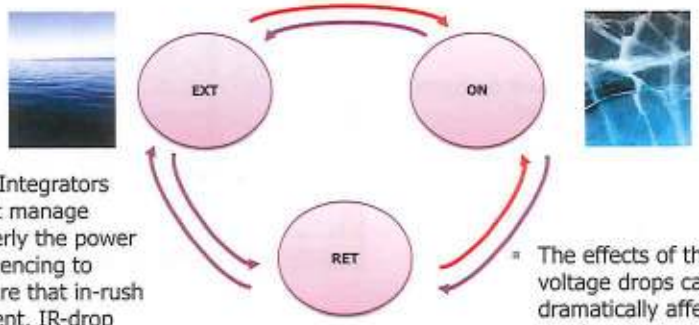
Challenges	Description	Existing methodology	Benefits of CLICK solution
	Determined by the power up sequence of power switch cells	**Daisy chain** Optimization of the power up sequence is iterative	**Transition Ramp Cell** Handling automated and right-on-first pass implementation of the power up sequencing of an islet
#1 Low Frequency IR Drop	Power management network must be sized to sustain voltage drops caused by in-rush current at mode transitions	Verification of the power up sequence can only be done after P&R Verification of the impact of voltage drops on power management network is long and performed after P&R	Fast **Mode Transition Check** simulation enabling Low-Frequency IR-drop analysis, to help in regulator sizing early in the flow
#2 Static IR Drop	Determined by power switch sizing and number	**Fuzzy guidelines** are usually delivered by IPs providers Power switch implementation is iterative	**Scripts** for automatic and optimized insertion of power switch Non need for iterations

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Why are voltage drops due to mode transitions so critical?

- Mode transitions inherent to partitioning of a SOC into islets cause voltage drops on the main power supply



- SoC Integrators must manage cleverly the power sequencing to ensure that in-rush current, IR-drop and wake up time are within an acceptable range
- The effects of these voltage drops can dramatically affect the functioning of the Soc

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Challenge #1
Low frequency IR Drop management

- **In-rush current** must be controlled in order to avoid excessive **low frequency IR Drop** in the power network by powering up inactive blocks in small increments (power-up sequence)
- Accordingly, the timing sequence of the control signals has to be defined carefully and verified through simulation
- There are two existing methodologies for power switch control: **daisy chain** and **high-fanout**
- To reduce in-rush current during power up, a daisy chain connection is generally preferred

The Transition Ramp Cell is the alternative

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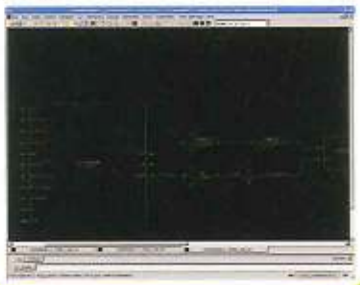
Power up sequence of the islet to manage low frequency IR Drop

Existing solution: Daisy chain

- Virtual supply rail connected by a **dual switch network** design
 - One providing the "soft start" as a daisy chain of weak "starter" power switches
 - Another, "main" network of strong power switches which turns on when the virtual rail reaches a predetermined trigger level
- **Several** dynamic rail analysis **iterations** required with variations of the number of switches, and turn-on timing interval
- Dual switch network requires **more wake up time**
- **Verification comes late** in the flow and is dependent on IR drop analysis tools

CLICK solution: TRC

- Virtual supply rail connected by a **single switch network** design for faster wake up time
- Combined with a **Transition Ramp Cell** to limit automatically the current flowing through the power switches



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Power up sequence of the islet to manage low frequency IR Drop

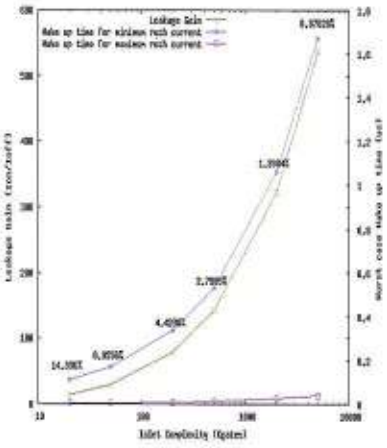
Benefits of a power up sequence with the TRC

- Only Single switches required, leading to **faster wake up time**
- No need for inverters/buffers for **higher density**
- SoC Integrator only has to specify the value of maximum in-rush current with the bus of the TRC
- Activity Control Unit **complexity is reduced** (isolation, retain/pwd signals handled by TRC)
- Configuration can be **dynamically changed** to fit to the different chip power states
- Iterative and complex Inrush current analysis is no more required as power up sequence is **guaranteed by design**
- **Automatic insertion** of the TRC by a script in the ring of power switches

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TRC configuration and integration

- The blue curve represents the wake up time for a scenario where TRC is configured to maintain the minimum in rush current depending on islet complexity
- Wake up time can be improved by 10 to 100 times if in rush current limit is relaxed!
- TRC area at TSMC 55 nm LP
 - 288 um2
 - Equivalent to only 5 power switches!



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New methodology to check drops due to mode transitions: « Mode Transition Check »

- **Simulation** enabling Low-Frequency IR-drop analysis dealing with power mode changes
- For sizing the regulator to the predefined islet, and/or sizing the islet for the selected regulator
 - Assessing the Dynamic IR-Drop and low frequency IR-Drop budgets,
 - Assessing wake-up time/Inrush current trade off,
 - Assessing the power islet consumption per mode, the capacitance and the resistance,
 - ...
- For optimizing regulator sizing

Early and fast simulation

✓ Verification by simulation of the sequencing of the islet handled by the TRC, to confirm the compatibility of the pair regulator sizing - in-rush current of the islet
✓ Only few minutes required for simulating an islet with its regulator

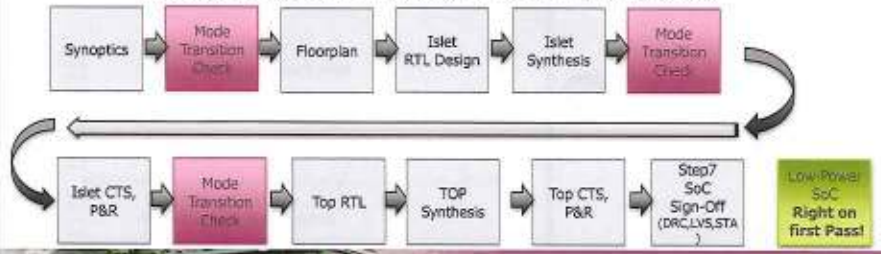
✓ No need for iterations as simulations with refined data are performed all along the flow

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MTC in the design flow

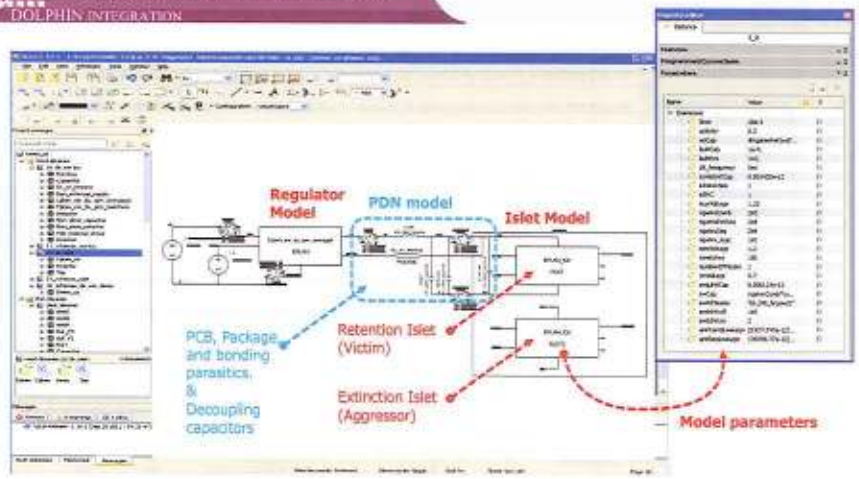
- **SPICE** transient analysis (short simulations thanks to behavioral models)
- Performed before **RTL** (rough estimation), after **synthesis** and after **P&R** (refined power consumption)
 - Starting with basic consumption metrics (power consumption as a function of an islet of a given size) at architectural level
 - And then using extractions with accuracy relative to the project progress



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Models required for MTC

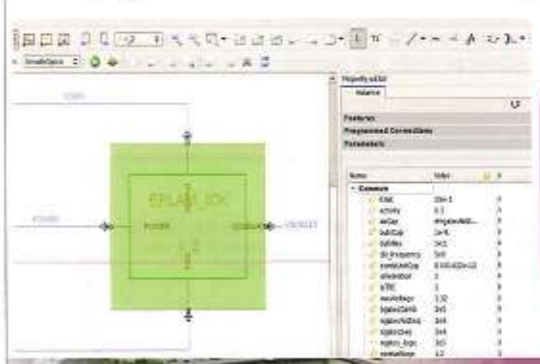


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Focus on the model for a power islet

- Technology dependent parameters
 - Internal capacitance
 - Leakage current profile per mode
 - Dynamic power consumption profile
 - …
- Application dependent parameters
 - Operating modes
 - Circuit size
 - Switch ratio
 - …



Easy usage

✓ Models with default parameters must be delivered by the library provider

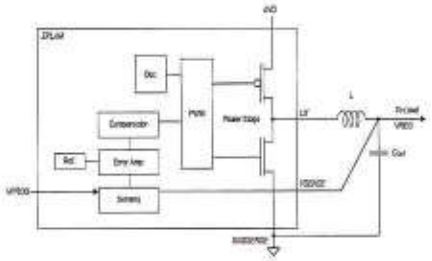
✓ Soc Integrator will tune the parameters according to the characteristics of the islet

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Focus on the model for a switching regulator

- Application dependent parameters
 - Maximum output current
 - Minimum drop out voltage
 - Line regulation
 - Load regulation
 - Load transient
 - …



Flexibility of models

✓ User can play with parameters and check easily the impact on mode transition drops

✓ After each simulation, models parameters are automatically updated with refined data

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Progressive verification with model refining

Power consumption analysis with mixed signal simulator



Post Synthesis: Results of power analysis based on post-synthesis netlist are available

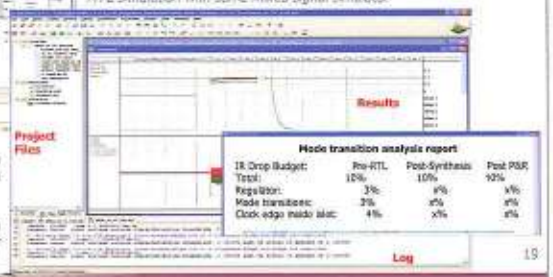
Post P&R: Results of power analysis based on post layout netlist and IR drop values are available

Instantiating models with Schematic Editor



Model parameters are automatically updated with extracted values

MTC simulation with same mixed signal simulator



Post Synthesis: Run synthesis with UPF file description as with traditional design flow, and combined it with power consumption simulation and MTC simulation

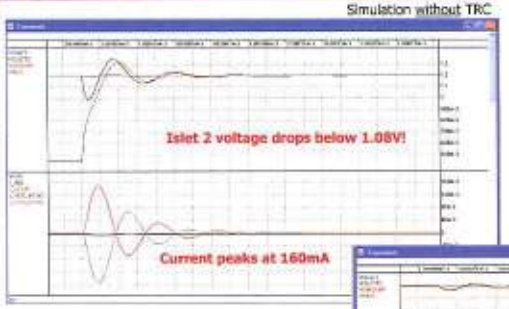
Post P&R: P&R with UPF/CPF file description as with traditional design flow, and combined it with power consumption simulation and MTC simulation

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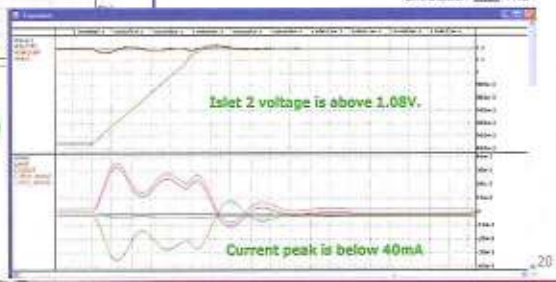
Demonstration with and *without TRC*

Simulation without TRC



VOLTAGE VIOLATIONS!

Simulation with TRC



NO VOLTAGE VIOLATIONS WHEN USING TRC!

Conditions
- TSMC 55 nm LP
- TT; 25° C

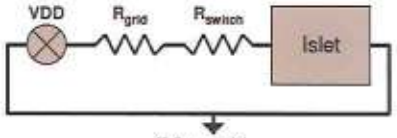
Operating modes
- Islet 2: RET
- Islet 3: EXT > ON

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Challenge #2
Static IR Drop management

- The **size** and **number** of power switches must ensure acceptable IR-drop during normal operation (ON)
 - To limit IR-drop, the resistivity of the power structure (power rail + power switches) must be as small as possible
 - Inserting a larger number of power switches minimizes the IR drop, but consumes more area and routing resources



IR Drop model

- The challenge is to find the optimal configuration!

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Static IR Drop management

Existing Solutions: user manual

1. **Manual estimation** of the number of switches based on targeted static IR Drop budget and power estimation or use of the "explore_power_switch" command
2. MaxIR drop summary for all configurations, selection of the appropriate power switch and placement pitch
3. Insertion of power switches based on standard P&R tool **command** "create_power_switch_ring" and "map_power_switch"
4. **Validation** of the power switch implementation **after P&R** with IR Drop analysis tools
5. If IR Drop budget is not respected, new manual estimation of the number of switches is required

Several iterations required to define the optimal number of switches

CLICK solution: scripts

1. Script for **automatic computation** of the number, sizing and insertion of power switches based on targeted static IR Drop budget, **without** need for **iterations** delivered by the IP provider

Inputs (can be extracted with MTC):
1. Current limit when powering-up the islet
2. The targeted static IR-drop
3. The average power consumption of the islet
4. The estimated islet capacitance

2. Based on standard P&R tool **command** "create_power_switch_ring" and "map_power_switch" for seamless integration within standard flow

3. **Script** for automatic optimization of power switches

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The construction quandary is solved!

THANK YOU !



Dolphin Integration is your partner for

- Providing Silicon IPs for low power SoCs from regulators to standard cell libraries
- Providing specific cells, models, scripts, methodologies of simulation for safer and easier implementation of power islets in a SoC

Contact
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Design and Implementation of High Resolution 60GHz PLLS and DCOs Using the EMX 3D EM Simulator

Integrand Software

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ABSTRACT

Frequency synthesis at mm-Waves is still dominated by analog PLLs, although all-digital PLLs (ADPLLs) have been widely explored below 10GHz. The major obstacle has been the poor quality of digitally controlled oscillators (DCO) as MOS varactor Q-factor drops to <10 at 60GHz. A mm-Wave digital transmitter (TX) based on a 60GHz fractional-N ADPLL with two-point FM is proposed here. To achieve a wide tuning range and raw ~1MHz resolution at 60GHz, a DCO with reconfigurable distributed metal capacitors and transformer attenuation of the frequency step is integrated by exploiting the multiple metal layers available in TSMC nanometer technologies. Shorting metal shield strip pairs beneath a transmission line (TL) increases its capacitance per unit length, thus introducing phase shift in the resonator and decreasing the oscillation frequency. Compared to a MOS varactor, distributed metal capacitors provide higher Q-factor, finer tuning-steps and fast design/layout turn-around time.

There are a number of challenges in the design and modeling of circuits at these frequencies involving both active and passive circuitry. In this paper we discuss some of the challenges and solutions for the modeling of passives at these high frequencies. As frequencies increase, the coupling between on chip passives becomes critical. For example isolation between different inductors on a chip becomes very important. In addition, stray interconnect lines surrounding sensitive passives can resonate once they become a fraction of a wave length. Dummy and metal fill can introduce significant loss in the system. Structures like MOM capacitors become the bottleneck for high frequency applications (instead of inductors). In this paper, we describe the use of the EMX 3D simulator to model these high frequency effects. We describe how the fast multipole method (FMM) algorithm can be very efficient for even solving the problems arising from the large problems and dense meshing that arise from the solution at high frequencies

For the implementation of the PLL and DCO extensive EM simulations on the complete DCO tank together with interconnections to the divider and PA are performed with the EMX simulator. EMX has the ability to accurate model all the passive circuitry including the inductors, distributed MOM capacitors and interconnect. This is particularly critical at 60GHz where complex component interaction needs to be modeled accurately.

The 60GHz ADPLL-based TX was fabricated in TSMC's 65nm 1P7M CMOS. The 2.2mm2 total die area includes bondpads, PA, SRAMs and other digital circuitry for debugging. The ADPLL core occupies 0.5mm2 and consumes 40mA (11mA DCO, 23mA prescaler, and 6mA for the rest) while the PA dissipates 34mA, both from a 1.2V supply. After de-embedding cable/probe losses, +5dBm into 50Ω is observed at the PA output with a gain flatness of 1dB across the 7GHz locking range (56.4 to 63.4GHz). A very low level FREF spur of -74dBc is measured in the 60GHz spectrum with virtually no other spurs observed. By dynamically changing the loop BW during acquisition, a good PN of -72dBc/Hz at 100kHz and -90dBc/Hz at 1MHz frequency offset is achieved at ~60GHz, while the loop settles within 3us.

Integrand Software, Inc.

Design and implementation of high resolution 60GHz PLLs and DCOs using the EMX 3D EM simulator

Sharad Kapur and David Long
Integrand Software, Inc.

Wanghua Wu, R.B. Staszewski and John R. Long
Delft University of Technology

Integrand Software, Inc.

Outline

- Introduction and motivation
- High frequency modeling and simulation
- mm-Wave DCO design
- 60GHz ADPLL design
- EMX modelling methodology
- Measurement results
- Conclusion

[1] W. Wu, J.R. Long, R.B. Staszewski, and J.J. Pekarik, "High-resolution 60-GHz DCOs with reconfigurable distributed metal capacitors in passive resonators," ***Proc. IEEE Radio Frequency Integrated Circuits Symp.***, pp. 91–94, June 2012.
[2] W. Wu, X. Bai, R.B. Staszewski, and J.R. Long, "A 56.4-63.4GHz spurious free all-digital fractional-N PLL in 65nm CMOS," ***IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers***, pp. 352–253, Feb. 2013.
[3] W. Wu, X. Bai, R.B. Staszewski, and J.R. Long, "A mm-wave FMCW radar transmitter based on a multirate ADPLL," ***Proc. IEEE Radio Frequency Integrated Circuits Symp.***, pp. 107–110, June 2013.

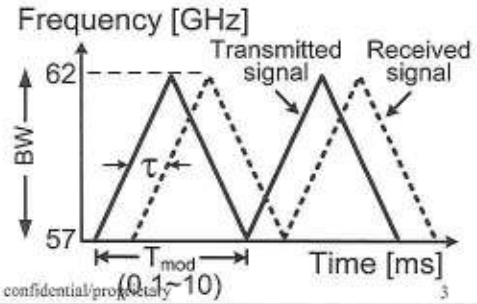
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mm-Wave Applications

- Gbit/s communications - WiGig v1, IEEE 802.15.3c, …
- mm-Wave imaging - industrial inspection and security
- **FMCW radar**: - high resolution in space and velocity
 - full 2D object detection

Range resolution:
- Large BW $\Delta R = \frac{c}{2BW}$
- Linear chirp

E.g., ΔR=3cm requires
BW=6GHz, linearity < 0.1%



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Challenges at 60GHz

- Modeling challenges
 - Full system EM simulation required
 - Interaction between components
 - Distributed effects are critical
 - Needs to be fast and accurate
 - Handled by Integrand
- Design implementation challenges
 - Circuit design with new passive architectures
 - Handled by Delft
- Manufacturing and fabrication challenges
 - Does the process meet the spec at 60GHz?
 - Handled by TSMC
 - 65nm/90nm RFCMOS process used

Modeling challenges at high frequencies

- Modeling of active devices
 - Transistor models (TSMC models upto 30GHz)
- Modeling of passive components
 - Largely dependent on the metallization and substrate
 - Does the foundry fabrication meet process specs?
- More detail on modeling passive structures and components at very high frequencies

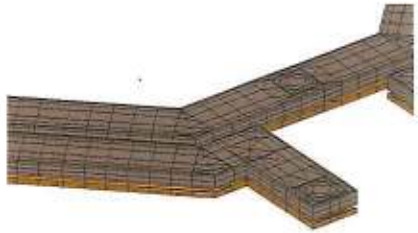
3D Planar EM Simulation

- **EMX®** is a 3D EM simulator
- 3D volume integral formulation (time-harmonic)
- Charges and currents unknown
 - Surface charges and volume currents
- Includes retardation (time of flight)
- Skin effect is critical at higher frequencies so you need a volume current and meshing of the metals

$$A(r) = \int G_A(r, r')J(r')\,dr'$$

$$\phi(r) = \int G_\phi(r, r')\rho(r')dr'$$

$$E_s(r) = \frac{1}{\sigma}J(r) + j\omega A(r) + \nabla\phi(r)$$



Accuracy (Electromagnetics)

- All physical effects included
 - R, L, C, substrate in a fully coupled manner
- Inductance
 - Distributed 3D volume currents
- Resistance
 - Skin effect and volume loss
- Capacitance
 - Accurate side-wall capacitance
 - MIM and thin-film capacitors
- Substrate
 - Multi layered lossy substrates
 - Substrate doping and bias
- Vias
 - Via inductance and capacitance

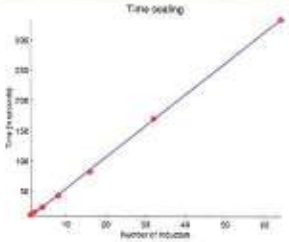
$$E_s(r) = \frac{1}{\sigma}J(r) + j\omega A(r) + \nabla\phi(r)$$

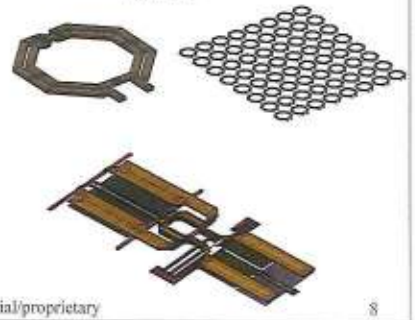




Speed (Numerics)

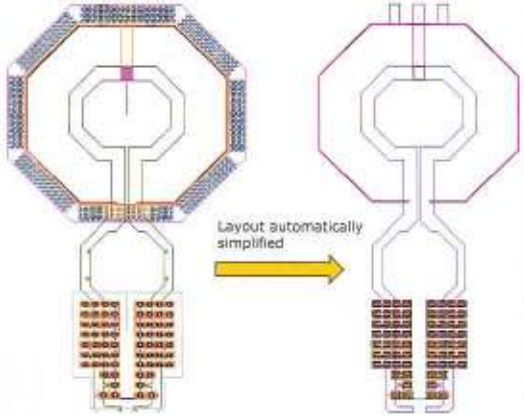
- Integral equation-based
- 3D EM field solver
 - Preconditioned iterative methods
 - New "Full-Wave" FMM
 - Adaptive Fast Frequency Sweep using Krylov subspace techniques
- Single inductor in a matter of seconds
- Large structures are now tractable





Easy to Use

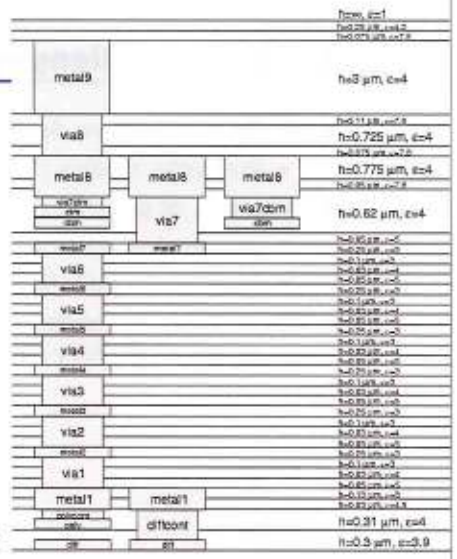
- EMX accepts true mask layout and will automatically simplify the layout for meshing and EM simulation
 - Via arrays, slotting rules, metal fill simplified
 - Boolean masking operations can be performed
 - Can apply grows and shrinks to the geometry including half-node scaling and metal bias
- **What goes to mask goes to simulator!**



Vias merged
Fill removed
Metal bias applied
MiM cap bank handled

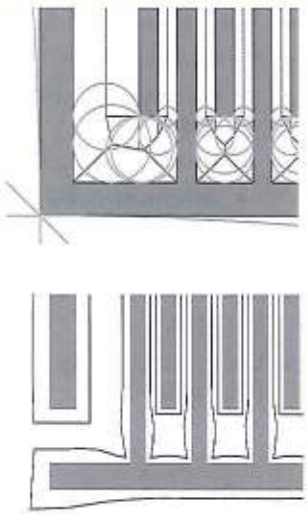
Generic 65nm Process

- Thick metals
 - ~3um copper
- High-resistivity substrates
 - 10 Ω-cm
- Fine feature sizes
 - 0.1μm width at 65nm
- Many metal layers
 - High density capacitors
- Easier for MOM/Integral solutions that do not need to "discretize" dielectric interfaces and only conductors



TSMC iRCX Technology Files

- Accurate process parameters are critical for EM simulation
- TSMC iRCX file provides a detailed process information
- Width and spacing dependence (paper at RFIC 09 with TSMC)
- These Voronoi diagrams are used to alter the drawn layout to mimic the fabrication process

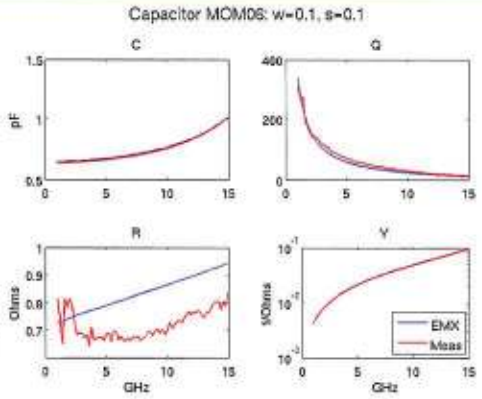


MOM (finger)Capacitor



3D mesh of 0.6pF Cap

Capacitor modeling critical for DCOs



Example	Ports	Freq Range	Size	1 CPU		8 CPUs	
				Mem.	Time	Mem.	Time
MoM capacitor	2	0.2GHz-20GHz	48,997	1140MB	19m12s	2591MB	5m59s

Courtesy: TSMC. 65nm RFCMOS, 9LM thick metal technology. Published at RFIC 2009
"Including Pattern-Dependent Effects in Electromagnetic Simulations of On-Chip Passive Components", Integrand and TSMC

Issues at High Frequencies

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- The skin effect is a significant
- Meshes need to be finer to incorporate these effects
- This leads to larger problem size (smaller structures?)



1GHz



1-micron mesh



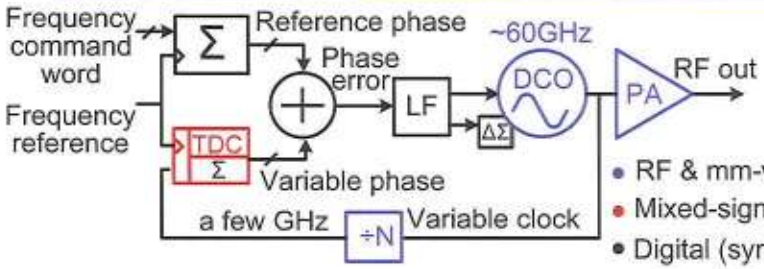
60GHz



0.1-micron mesh

60GHz ADPLL Challenges

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- Lack of mm-wave DCO:
 → high freq. resolution, wide tuning range, low PN
- Integration effort: mm-wave + RF + analog + digital
 → overall system performance ?
- Wideband FM traverse entire DCO tuning range
 → k_{DCO} calibration and linearization

New Tuning Method for mm-Wave DCO

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Target: 6GHz linear mod. range & ~2MHz tuning step

- MOS varactor-based tuning bank at mm-wave freq.
 - low-Q (e.g., 50fF@ 60GHz, Q= ~5)
 - limited freq. tuning step ~10 MHz and range <10%
 - sensitive to PVT
- **Digitally-reconfigurable passive resonator**

 Embed distributed metal capacitor in a passive resonator: **inductor, transformer, transmission line**



Digitally-Controlled Passive Resonators

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- Exploits multiple metal layers in CMOS
- Digitally control resonators via distributed metal cap. + MOS switch → DCO tuning steps can be easily calibrated
- Parasitics of interconnection observed in passive resonators → achieve wide tuning range and high-Q
- Full-tank EM sim. increases first time right chance
 → not rely on varactor model
- New method is proposed for fine tuning at 60GHz→

 Transformer-based DCO (T-DCO)

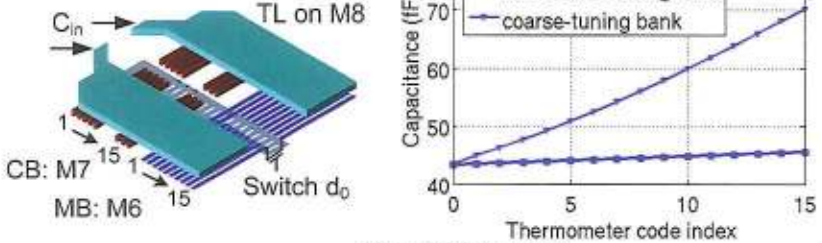


Principle of Coarse Tuning

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Differential transmission line with switchable metal shield

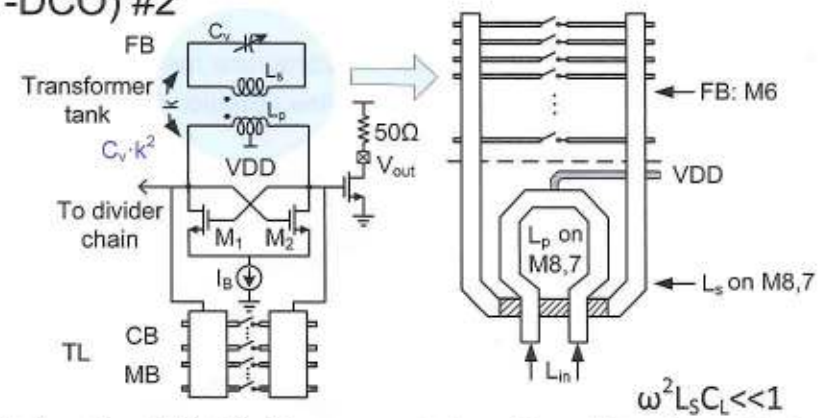
- Shorting strips via MOS switches → increase cap. per unit length and phase shift along TL, reduce tank resonant freq.
- Placing shielding strips at various metal layers → coarse and mid-coarse tuning bank



60-GHz Transformer-based Fine-tuning DCO

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(T-DCO) #2



- Placing the FB (C_V) at L_s
- C_V attenuated by $k_m^2 L_s/L_p$

$\omega^2 L_S C_L << 1$

- C_V is unit-weighted cap. Bank → linear fine-tuning (~2MHz)

60 GHz DCO Design Methodology

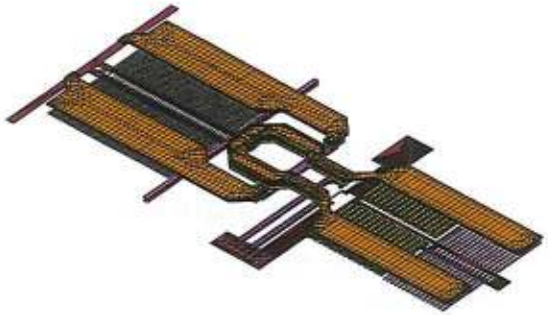
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- 1. Specify L, C, and ΔC for targeted tuning step and range
- 2. Design capacitor bank for coarse-tuning:
 - Capture TL prototype based on initial spec.
 - Generate N-port S-parameter data from EMX
 - Use S-parameter data to verify frequency and tuning range
 - Adjust TL dimensions (if required) to meet target spec.
 - Fit S-parameter data to lumped-circuit model
- 3. Repeat step 2 for the transformer design
- 4. Add ground plane, interconnections, etc., to verify their influence. Adjust design as necessary to meet spec.
- 5. Full-EM simulation of tank (L and C together) as final verification.

Full DCO Tank Simulation in EMX

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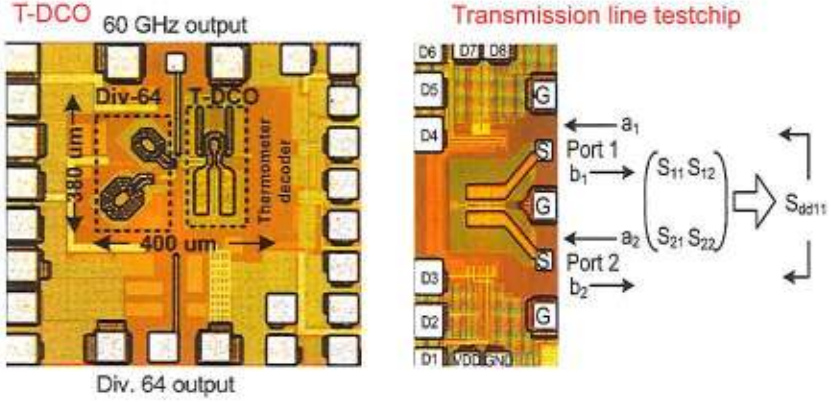
- EMX simulation of 60GHz DCO
 - TL-based coarse and mid-coarse tuning bank, transformer based interconnect, ground plane
 - Ports: 175
 - Layout size 400x200μm²
 - Computational resources
 - 3GB memory
 - 8 CPU (2.2GHz)
 - 6 hours of sim time



60-GHz DCO Test Chips

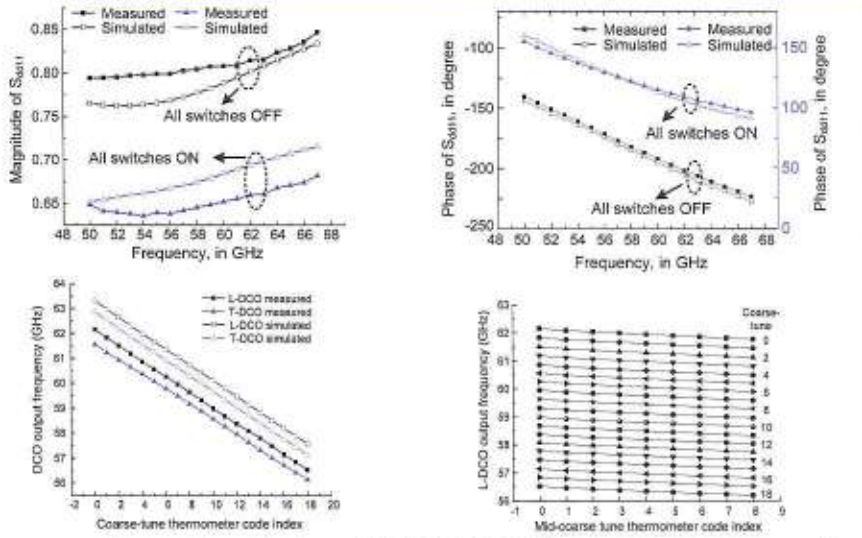
Integrand Software, Inc.

[published at RFIC 2012]



Measured Results

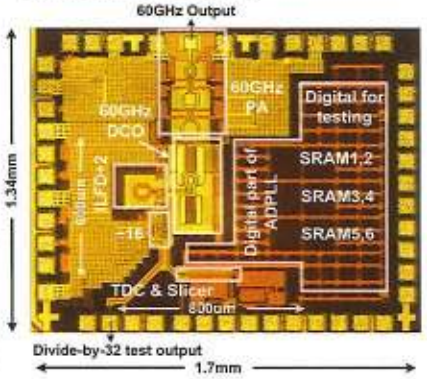
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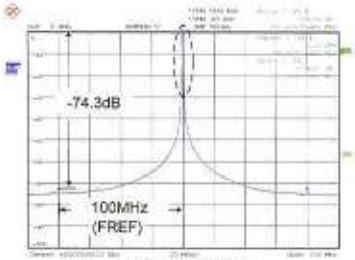


60GHz ADPLL

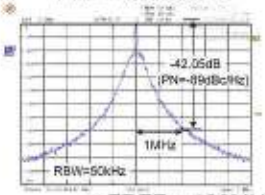
TSMC 65nm CMOS

[W.Wu ISSCC 2013]





- f_{out} = 60.0209GHz
- PN = -89 dBc/Hz



- FREF = 100MHz
- Reference spur = -74.3dBc

Performance Summary

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COMPARISON OF STATE-OF-ART OSCILLATORS ABOVE 50 GHZ

Ref.	Type	F_0 (GHz)	FTR (%)	F_{res}	PN (dBc/Hz)	P_{DC} (mW)	FoM_T (dBc/Hz)	CMOS
[3]	DCO	58.27-63.83	9.5	2.3 bit	−90.1	10.6	−174.9	90 nm
[4]	DCO	51.3-53.3	4	10 bit 1.8 MHz	−116.5[1]	2.34	−179.2	90 nm
[9]	VCO	56-60.35	7.4	NA	−95	22(IQ)	−174	65 nm
[10]	VCO[2]	57-66	14.6	NA	−75	28(IQ)	−159.5	45 nm
L-DCO	DCO	56.22-62.16	10	12 bit 160 kHz	−93	12	−177.9	90 nm
T-DCO	DCO	55.83-61.55	9.75	12 bit 2.5 MHz	−94	14	−177.9	90 nm

[1] PN @ Δf=10 MHz, the rest are at 1 MHz. [2] High/low-band two VCOs.
$FoM_T = PN - 20\log_{10}(F_0/\Delta f \cdot FTR/10) + 10\log_{10}(P_{DC}/1mW)$

DCO performance

	This Work	ISSCC'09	JSSC'11	ISSCC'08	TCAS-I'11	
CMOS	65nm	45nm	90nm	65nm	90nm	
Center frequency	60GHz	61.5GHz	60.5GHz	33GHz	40GHz	
Architecture	TDC-ADPLL	Charge pump analog PLL	20GHz analog PLL x 3	BB-ADPLL	BB-ADPLL	
Type	Fractional-N	Integer-N	Integer-N	Integer-N	Integer-N	
Reference freq.	10...100MHz	10MHz	39MHz	275MHz	156.25MHz	
Phase noise (1kHz)	at-100kHz	-72dBc/Hz	-71.5dBc/Hz	-63.6dBc/Hz	NA	-73dBc/Hz
	at-1MHz	-90dBc/Hz	-75dBc/Hz	-95dBc/Hz	NA	-93.67dBc/Hz
FREF spur	-74dBc	-42dB	-67~-58dBc @20GHz	NA	-48dB	
Frequency range	7GHz (11.6%)	5GHz [s/b, 2 VCOs] (14.6%)[1]	5GHz (8.3%)	6GHz (20%)	3GHz (7.5%)	
Power consumption	48mW(1.2V)	78mW (1.1V)[1]	80mW (1.2V)[1]	64mW(1.8V) 1.1V)	48mW(1.2V)	
Core area	0.48mm^2	0.52mm^2 [with pad]	1.68+0.2mm^2 [2 G-to, with pad]	NA	0.3mm^2	

* Provide quadrature outputs at 60GHz.
[1] PLL locking range is 2.4GHz, limited by injection locking divider's locking range.

ADPLL performance

Conclusions

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- Design and implementation of novel 60GHz circuits like DCOs and ADPLLs
 - High resolution mm-wave DCO using novel passive resonator structures that use CMOS metal layers to tune circuits
 - Excellent RF performance for ADPLL, low phase noise, low power and small chip area
- Implemented in TSMC 65nm CMOS
- First pass design using full system EM simulation with EMX
- Excellent simulation to measurement correlation

Not confidential/proprietary

NOTE

Soft-Error Testing at Advanced Technology Nodes

GUC

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

With latest advances in semiconductor manufacturing, novel soft error failure mechanisms may emerge that will dominate FIT rates. The biggest challenge faced by individual semiconductor companies is the cost of evaluating a circuit design for such failures in a fabrication process that is not yet commercially available. Additionally, TSMC is reluctant to grant access to a process that is not yet production-ready. To achieve early understanding of these failure mechanisms at advanced technology nodes, designers must collaborate with TSMC to develop failure models for mitigation. GUC, Cisco Systems and Vanderbilt University, along with other industry partners, have jointly developed such a collaborative program for soft error analysis in advanced technologies. This presentation will detail the goals of this collaborative effort along with logistical issues faced by such a consortium for addressing failure mechanisms that are going to be a major issue for future technologies.

Novel physical mechanisms for soft-error failures are emerging with scaling, such as charge-sharing, which complicate the modeling, testing, and design issues faced by the industry. As part of this project, a test-IC concept is developed where all partners pitch in to pay for access to the fabrication process. TSMC grants the access since it will receive necessary data related to soft errors for adjustment in their process. Information available from the test IC will help designers understand effects of novel mechanisms on their circuit designs, and provide enough details to estimate FIT rates of their products.

GUC-Cisco-TSMC-Vanderbilt team along with five industry partners started the project at 28 nm technology node and three more companies joined for the 20nm project which tapeout this Feb. The primary goal of the project is to identify soft-error failure modes and develop mitigation strategies. The design of the test IC is carried out by Vanderbilt University with different cell designs from each partner that needed evaluations. These cell designs are placed in an appropriate test structure (a shift register for flip-flop designs, a Combinational-CREST design for combinational logic circuits, etc.). A common set of test structures that can be used as baseline for everyone was also designed and implemented. GUC carried out custom layout and physical design of the test ICs. Functional testing followed by irradiation testing with neutron, alpha and heavy-ion particles was also carried out. The presentation will focus on the collaborative effort for addressing future reliability challenges in 20nm and beyond.

GUC
The Flexible ASIC Leader

Soft-Error Testing at Advanced Technology Nodes

Kuoshu Chiu
GUC

Outline

- Collaboration project background
- Project information
- 20nm design tape-out
- Summary

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Why Soft Errors?

- Soft errors will dominate future FIT rates
- Uncertainties and difficulties involved in soft-error modeling require a proactive approach to understand effects of design and fabrication process on FIT rates
- For advanced technologies, factors affecting soft-error rates range from process parameters to environment to design parameters
- Effectiveness of soft-error mitigation schemes are not clear at advanced technologies



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Soft-Error Impact: Industry Perspective

Soft errors will dominate future FIT rates

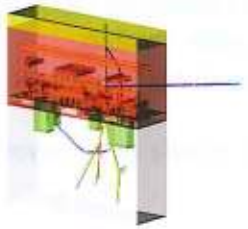
- **Cell phone with one 4-Gbit, low-power memory with an SER of 1000 FITs per megabit**
 - One soft error every 10 days
- **High-end router with 100 Gbits of SRAM with SER of 600 FIT/MB**
 - One error every 17 hours
- **Router farm that uses 1000 Gbits of memory with 600 FIT/MB**
 - One potential network interruption error every 1.7 hours
- **Trans-Atlantic airline passenger at 35,000 ft working on a 2 Gbits SRAM memory laptop**
 - A FIT/MB SER 100,000 FIT/MB
 - One potential error every five hours

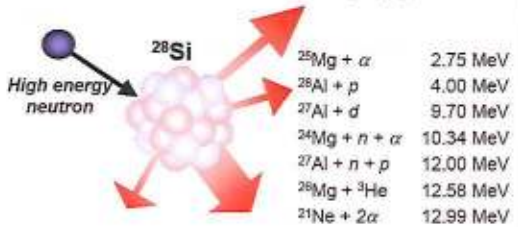
Mastipuram and Wee, – *EDN*, 9/30/2004

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Neutron Secondary Reactions

- **Neutrons react with silicon atoms to produce secondary particles**





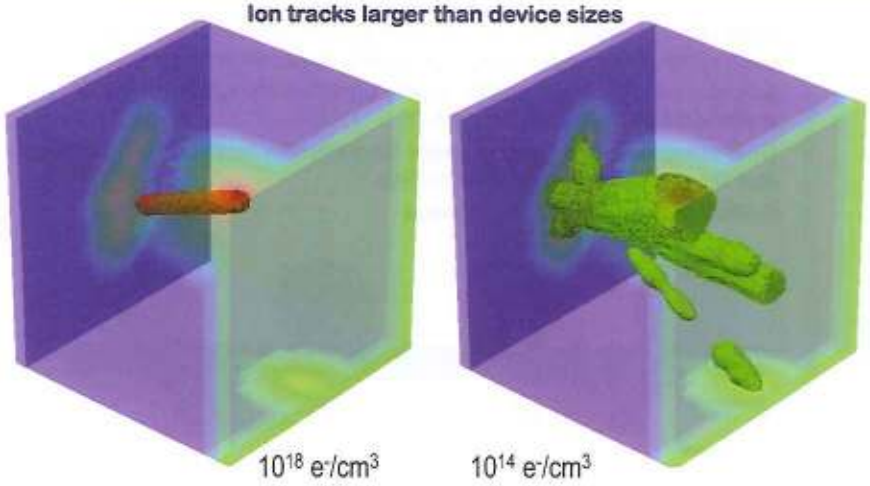
$^{25}Mg + \alpha$	2.75 MeV
$^{28}Al + p$	4.00 MeV
$^{27}Al + d$	9.70 MeV
$^{24}Mg + n + \alpha$	10.34 MeV
$^{27}Al + n + p$	12.00 MeV
$^{26}Mg + ^{3}He$	12.58 MeV
$^{21}Ne + 2\alpha$	12.99 MeV

NSREC short course, 2005

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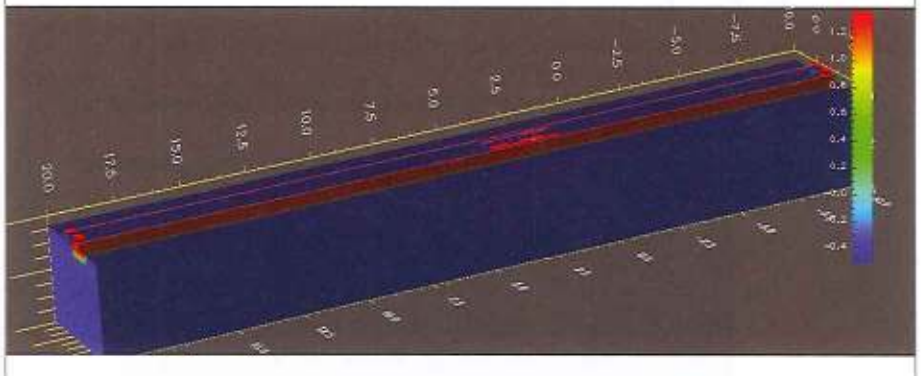
Single Event Silicon Effects

Ion tracks larger than device sizes



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E-Field Perturbation

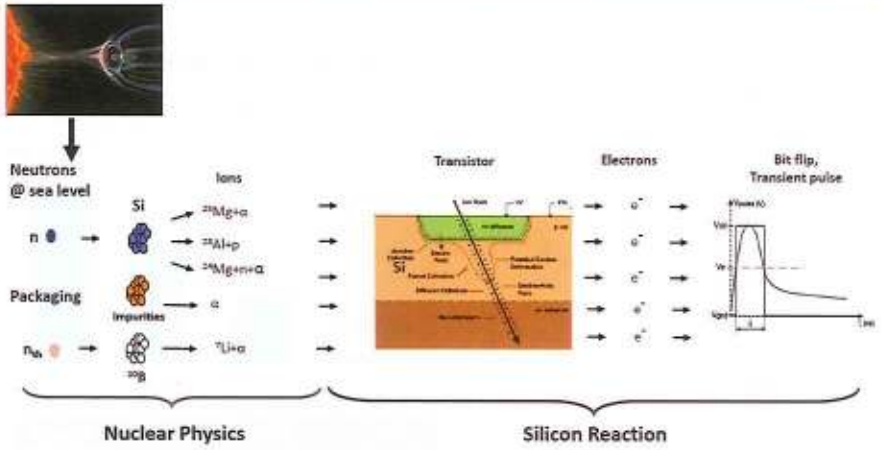


Perturbation in E field at 40 nm technology node as a result of an ion hit

Courtesy Robust Chip, Inc.

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The Soft Error/ SER Problem

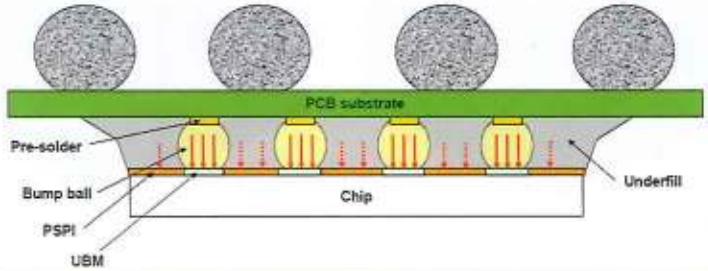


Understanding the Phenomena Requires a Combination of Nuclear Physics & Semiconductor Device Physics

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Alpha Particles Contamination Issues

- Alpha particles are generated by traces of radioactive material in the packaging. They have a very high ability to generate upsets.
- Industry requirements call for low to ultra low alpha emissions of materials (.01 to .002 alpha/cm2/hr)
- Chip manufacturers need to verify the emission level of their package and the immunization of their design.
- Critical mostly in flip chip package



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Designers Perspective

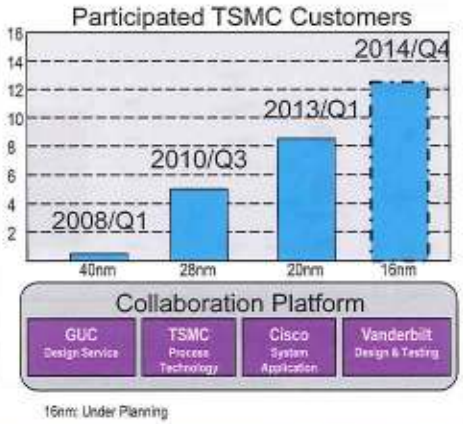
- Designers currently use data from two generations back to estimate FIT rates for soft errors
 - For 28 nm designs, designers are using 65 nm or earlier data
- Charge generation, transport, and collection mechanisms during a soft-error event *evolving* with scaling
- Data from older technologies may not be applicable to newer technologies
 - For example, DICE FF is no longer a reliable option beyond 40 nm technology

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Soft Error Rate Common Testing Platform

- Soft errors will dominate chip FIT rate
- Collaboration platform provides effective design learning and development



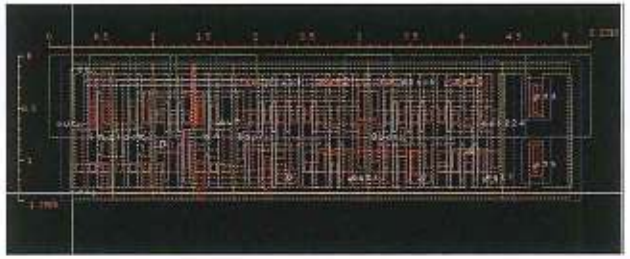


16nm: Under Planning

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Test IC Design

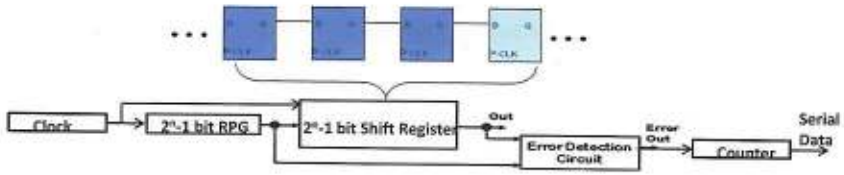
- Main objective of evaluating soft-error vulnerability of flip-flop designs from partners
 - CREST approach is used where flip-flops from partners are dropped blindly into a test circuit
 - Layout area and ports for flip-flop designs agreed upon in advance for all partners
 - Within the layout area, Individual companies can design whatever they want



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Test IC Design

- Overall test structure is identical, individual flip-flops are proprietary
- Baseline flip-flops (DFF and DICE FF) for comparison are added for everyone
- Vanderbilt and GUC integrated all flip-flops on test IC
- Targets TSMC processes for all designs



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Test IC Testing

- Alpha particle exposures were carried out at Vanderbilt University
 - Vary V_{dd}, temperature, frequency
- Neutron exposures were carried out at LANSCE, TRIUMF, and TSL
- Heavy-ion testing was carried out at LBNL and Brookhaven laboratories
- Proton testing was carried out at TIRUMF
- May take up to two years to complete all testing!

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Disposal

- Test ICs contain proprietary information from each partner
- Test ICs are disposed off properly after testing



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40nm Technology Node

- Vanderbilt University, Cisco Systems, Bayview, CertiChips, GUC and TSMC started the collaborative efforts
- 3 mm X 3 mm test IC
- Radiation exposures for neutrons, alpha, heavy-ion, thermal neutrons, protons, and muons carried out
- Resulted in 23 papers/presentations, 2 best paper awards at conference

CISCO VANDERBILT School of Engineering tsmc GUC The Flexible ASIC Leader

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40nm Node: Alpha Test Results (FIT/MB)

- Alpha source flux was $3.0x10^4$ particles/cm^2/sec
- Total influence was $2.592x10^9$ particles/cm^2 over 24 hours
- FIT rates are calculated for 0.002 particles/cm^2/hour
- Maximum observed standard deviation was ±0.15%

Name	Description	Vdd in mV				
		809	842	870	902	927
DFF	Standard – Inverter, TG	1343	1251	1130	1059	976
DICE	Hardness by redundancy	154	138	128	110	106
FF1	Low power version of DFF	407	346	283	240	216
FF2	High speed DFF– low V_{th} devices	1138	1107	1031	1009	962
FF3	DFF with NAND gates	1149	1102	1043	1000	957
FF4	Low power version of DFF	1630	1530	1461	1384	1333
FF5	High speed version of DFF	1094	1018	904	870	792

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40nm Node: Alpha Test Results (FIT/MB)

- Alpha source flux was 3.0x104 particles/cm2/sec
- Total influence was 2.592x109 particles/cm2 over 24 hours
- FIT rates are calculated for 0.002 particles/cm2/hour
- Maximum observed standard deviation was ±0.12%

Name	Description	Temperature in °C		
		25	50	75
DFF	Standard – Inverter, TG	1004	1101	1306
DICE	Hardness by redundancy	160	220	281
FF1	Low power version of DFF	323	366	495
FF2	High speed DFF– low V_{th} devices	818	889	931
FF3	DFF with NAND gates	839	883	972
FF4	Low power version of DFF	1213	1344	1432
FF5	High speed version of DFF	900	970	1106

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40nm Node: Neutron Testing @ LANSCE

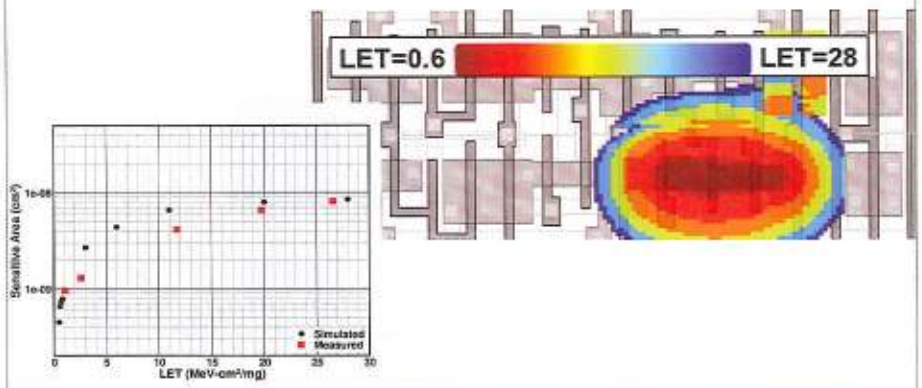
- Total neutron flux
 - 4889489 for input 1
 - 4512000 for input 0

Name	Description	Input 1		Input 0	
		Errors	FIT/MB	Errors	FIT/MB
DFF	Standard – Inverter, TG	122	269	95	225
DICE	Hardness by redundancy	67	147	51	121
FF1	Low power version of DFF	63	139	32	76
FF2	High speed DFF– low V_{th} devices	92	203	117	277
FF3	DFF with NAND gates	101	222	89	211
FF4	Low power version of DFF	115	253	105	249
FF5	High speed version of DFF	116	255	77	183

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Sensitive Area Simulation

- Sensitive area simulations identify the region on the layout that is sensitive to a given particle
- Analysis allows designers to develop precise mitigation techniques for optimum performance



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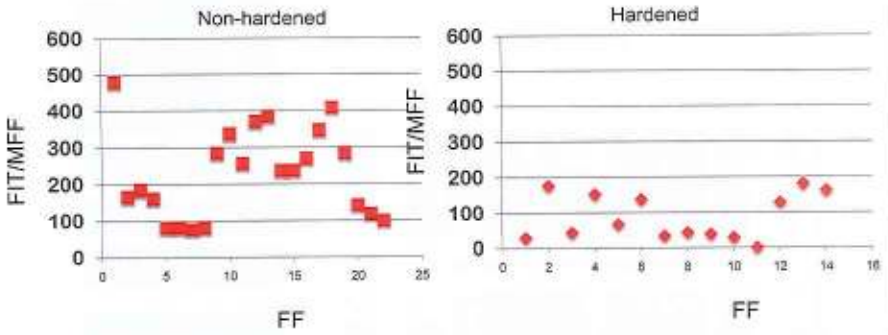
28 m Technology Node

- For 28nm technology, 7 industry partners joined the collaborative efforts
- 2 separate 3 mm X 2 mm ICs were designed
- On-going testing and data analysis for neutron, alpha, proton, and heavy-ion exposures

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28nm Node: Non-hardened vs. Hardened

- The difference in cross-section is less than an order of magnitude for neutron irradiations



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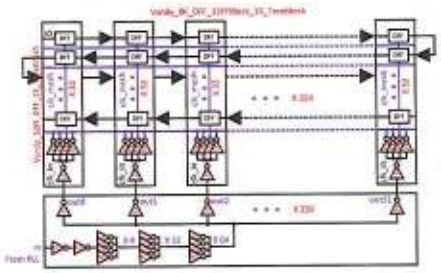
20nm Technology Node

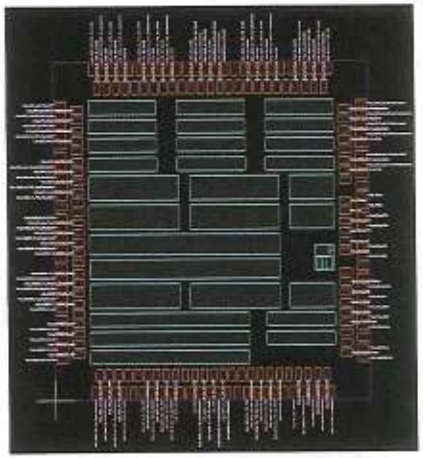
- For the 20 nm technology node, 10 industry partners joined the collaborative efforts
- 3 separate 2 mm X 2 mm ICs were designed
- Fab out date is August 5, 2013
- Neutron, Alpha, Proton, Heavy-Ion tests planned

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20nm Design Information

- Tapeout in 2013 Feb
- Fabout in 2013 Aug
- Chip size : 2000 X 2000 um
- Core area : 1700 X 1700 um
 I/O height 100 ~ 150um
- PAD pitch is 60 um.





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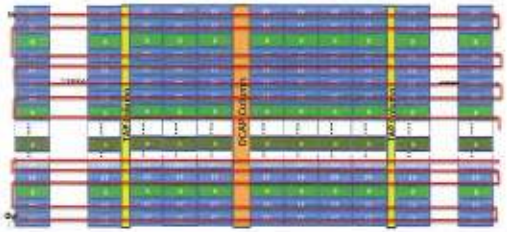
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Design Flow

- **Bottom up approach**
 - Taped out 3 chips with each chip contains 28 blocks.
 - There are 84 different FF designs
- **Run time**

Stage	CPU Time	Memory	Denote
Placement	00:15:15	2803M	~ 65K instances
Routing	03:21:30	4091M	EDI 11.13-e077
Extraction	00:05:34	2073M	~64K nets
DRC	31 hours	65988M	

* Machine: Red Hat 5.6 with 64G memory





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The Innovation – Double Patterning

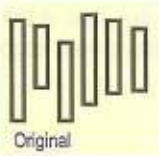
- **Double patterning**
 - Splits the layer into two separate masks, and each mask is exposed separately.
 - This technology is needed to get current 193nm lithography equipment to print correctly when metal pitches are below 80nm.

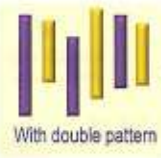
Geometry features disappearing due to lithography distortion

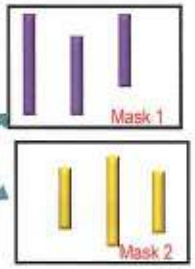


Not feasible due to optical resolution limits

Conventional Lithography







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Additional 20nm Requirements

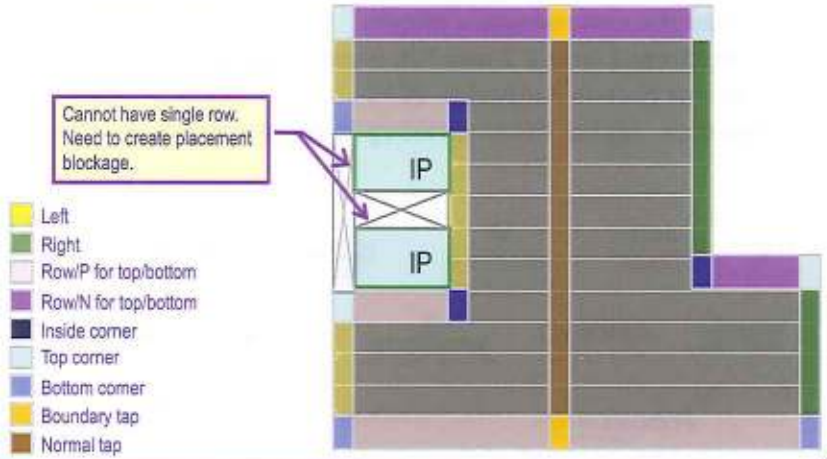
Implementation	•Floor Plan: -New boundary cell for L/R, T/B, and corner. - Colorize power plan and pin assignment for hierarchical design. •Placement: – Avoid potential color conflicts on cell abutment. – Placement to honor Vt min. area constraint. •Routing: –DPT aware routing. –Colorizing aware routing for colorized IP pin. – Delta voltage dependent spacing rule.
RC Extraction	•Extraction model for MEOL structure •DPT aware RC extraction •DPT misalignment effect RC tech. file •Generate multi-value SPEF
Timing Analysis	•Support reading multi-value SPEF •Additional Cap adjustment for setup/hold timing to account for DPT misalignment
Physical Verification	•Same mask spacing (G0) and different mask spacing check •Pre-color legality check
DFM	•New MEOL/BEOL type of ICOVL cell •DPT aware dummy insertion •LPC with DPT aware patterning matching

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Implementation – Floor Plan (1/2)

- Specific boundary cells for left, right, top, bottom, and corner.
- Different TAP cell for boundary and core area.



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Implementation – Floor Plan (2/2)

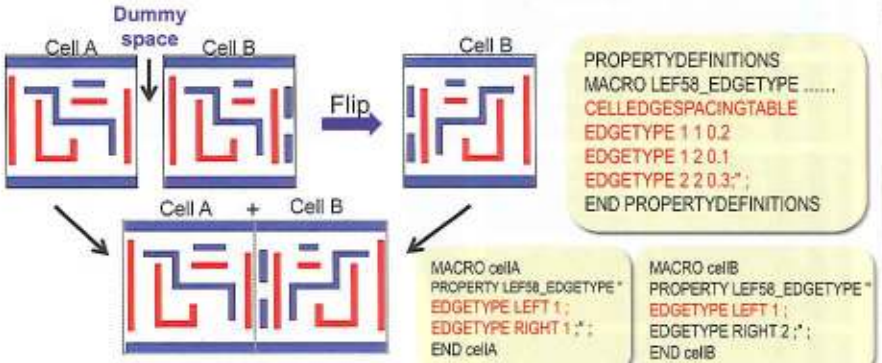
- **Colorize power plan and pin assignment for hierarchical design**
 - Colorization is done at the top level.
 - Push down the color constraint to each partition.
 - Honor color constraints in block implementation.
- **IP can have coloring attribute on pin shape. (defined in LEF)**
 - The color constraints on the block pins can be set by:
 - setAttribute –net $net –mask 1 …

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Implementation – Placement

- **Avoid potential color conflicts on cell abutment**



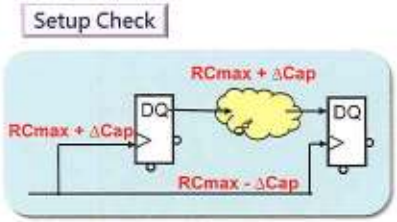
Edges are characterized so the placer knows if it should flip or inject a space.

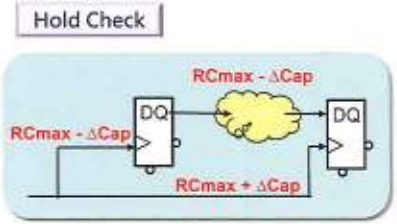
P30

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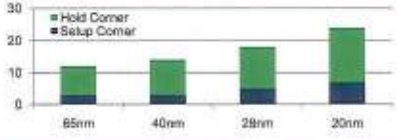
Timing Analysis: Consider Cap OCV

- **Additional cap variation due to DPT misalignment is considered for conservative setup/hold timing**
 - Each net should have multiple cap values in each RC corner





Process	Setup Corner	Hold Corner
65nm	3	9
40nm	3	11
28nm	5	13
20nm	7	17



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Summary

- **New 20nm manufacture techniques significantly increases design and integration complexity**
 - Fundamental design flow and tool changes
- **Tighter collaboration among designer, EDA vender, research and foundry can minimize the design risk**
- **The joint collaboration platform for SEU demonstrates how similar projects can reduce soft error FIT rates by orders of magnitude without significant performance penalty**
- **The collaboration will continue at 16nm and beyond**

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GUC Implementation Methodology & Tape-Outs

Advanced Technology
TSMC 40nm/28nm/20nm/16nm

High Gate Count Design
100M Gates Design, GHz Timing Closure

PPA Optimization
Low Power, High Performance, Compact Area

Variation Management Kit

Design for Reliability



- TSMC 20nm test chip tapeout
- TSMC 28nm design momentum
- TSMC 40nm mass production

- ***Over 500 projects have been production proven !!!***

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NOTE

An Efficient and Accurate Sign-Off Simulation Methodology for High-Performance CMOS Image Sensors

Berkeley Design Automation & Forza Silicon

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

This paper presents the challenges involved in achieving accurate, sign-off level simulations of high-performance image sensors, and discusses the simulation methodology developed at Forza Silicon using the Berkeley Design Automation Analog FastSPICE Platform to address these challenges. Many image sensor performance-limiting factors appear only when all of the active and passive devices in the array are modeled, including random device noise and layout parasitics. Coupled with the highly sensitive nature of image sensors, where tens of microvolts of noise can create noticeable image artifacts, this creates an enormous challenge for analog simulation tools, pushing both the accuracy and capacity simultaneously.

To address these challenges, our methodology uses a hierarchy of models for the image sensor blocks. At higher levels of the hierarchy, the complexity of the model is reduced, but the accuracy of the global interactions between blocks is maintained as much as possible. With the ability to tailor our model complexity for a desired simulation, we gain the advantage of rapid, accurate validation while keeping simulation time and resources manageable. Several capabilities found in the AFS Platform, qualified on the latest TSMC Custom Design Reference Flow, have significantly improved our verification flow. The AFS Full-Spectrum Device Noise subflow validates that our sensitive ADCs and readout chain will withstand the impact of device noise and parasitics. For top-level sign-off, AFS AMS enables us to speed up verification by using Verilog to model non accuracy-critical circuits while maintaining nanometer SPICE accuracy on blocks that were independently verified in other tools. Coincidently, AFS Mega has the required capacity, speed, and accuracy required for us to perform a final validation of our full top-level designs at the transistor level, including extracted parasitics.

In this comprehensive flow, device and circuit variability is also extremely important to image sensor performance and yield. Due to their highly parallel nature, Monte Carlo-based characterization allows us to predict image sensor nonuniformity due to device mismatch. Additionally, the AFS Circuit-Specific Corners subflow efficiently eliminates the limitations of traditional digital process corners and generates circuit-specific corners for each measurement that are suitable for analog designs. Reuse of these corners allows us to iterate critical circuits rapidly and confidently without the necessity of full PVT runs.

An Efficient and Accurate Sign-Off Simulation Methodology for High-Performance CMOS Image Sensors

Dr. Daniel Van Blerkom, Forza Silicon
Dr. Ravi Subramanian, Berkeley Design Automation

October 1, 2013

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Introduction

- Sign-off simulation methodology for CMOS image sensors
- Three way collaboration between
 - Forza Silicon: Image sensor design and development
 - TSMC: CMOS process with silicon-accurate models
 - BDA: Analog FastSPICE™ Platform

FORZA

tsmc Open Innovation Platform®

berkeley design automation, inc.

Forza Silicon Expertise

- Ultra-high resolution sensor design (208 megapixel)
- Low cost, low power, small-format sensors (1/7 in. form)
- Complete digital cameras-on-chip
- Ultra-small pixels with proprietary small-pitch column ADCs
- Custom infrared ROIC design
- Highly-integrated mixed-signal technology and SoCs



Automotive HDR Image Sensor



Stereo Sensor for Robotic Surgery



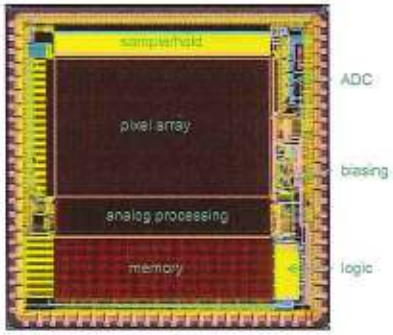
208 Mpixel Sensor

Forza Silicon Target Markets

- Low-cost, low-power
 - Smartphone cameras, digital camcorders, digital still cameras
 - Automotive, PC, security cameras
- High-performance, custom integration
 - Industrial automation, machine-vision systems, medical devices, professional imaging
 - OSCAR®-winning cinematography, rad-hard satellite imaging, defense
- High-speed I/O
 - Communications, computing



CMOS Image Sensors



- CCDs prior dominant imaging technology
 - Inflexible, require significant support electronics
- Integrates pixels into CMOS IC process flow enabling "camera on a chip"
- Sensor can include ADCs, memory, logic, RF, etc.

What Makes Sensor Design Different?

- Optical as well as electrical device
 - 3-D interactions important
 - Additional optical system requirements
- Highly engineered pixel design
 - 3-D structure, implant interactions & alignments
- Very sensitive analog circuit
 - To both electrical noise & temperature
 - Also extremely sensitive to uniformity
- High bandwidth data output
- Image quality has subjective component

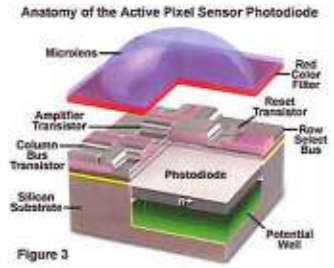
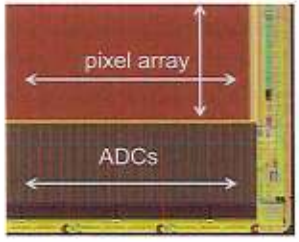


Image Sensor Design Issues

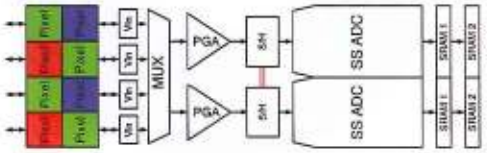
- Arrays of pixels, arrays of signal chains
 - Device matching
 - Supply and ground distribution
 - Control line routing
 - Extracting, managing and shielding parasitics
 - Managing switching currents
 - Cross-talk
 - Avoiding row correlated dependence
- Avoid abrupt boundary conditions
 - Dummy devices in layout
 - Timing always the same



CMOS Image Sensor Verification Challenges

- Simulating full design with all pixels at transistor level is impractical
- Simulation requirements extend from bottom to top of design hierarchy
 - Need accurate device noise analysis of pixel and analog signal chain
 - Need extensive analog signal chain characterization (e.g., corners and mismatch)
 - Need accurate simulation of many signal chains to predict fixed pattern noise
 - Need mixed-signal simulation of full-circuit image sensor
 - Need to include layout parasitics and device noise
 - Need high-performance for long multi-rate simulations

Analog Signal Chain



Sign-off Simulation Methodology

- Forza implements a hierarchical simulation plan
 - Block level and multi-block level to look at cross-talk
 - "cut-down" full chip level – parasitics but not all devices
 - Full chip with behavioral models
 - Verilog® sensor model
- Major verification areas
 - Pixel characterization and device noise analyses
 - Single Analog signal chain characterization
 - Many analog signal chains verification
 - Full-chip verification with sensor model

Verilog Sensor Model

- Speeds up application development
- Provides a way to model sensor performance in customer's system
- Checks interfaces and timing
- Output options
 - Image sequences
 - Row & column number data
- Verify integration time, gain settings, color order, etc.
- General application based on standard Verilog implementation



The Verification Platform

Forza Semiconductor Selects Analog FastSPICE™ (AFS) Platform



AFS Platform in Forza Verification Flow

- AFS Full-Spectrum Device Noise
 - Qualified in latest TSMC Custom Design Reference Flow
 - Pixel characterization
 - Analog chain characterization with device noise and parasitics
- ACE Characterization and AFS Circuit-Specific Corners
 - Qualified in latest TSMC Custom Design Reference Flow
 - Eliminates the limitations of traditional digital process corners
 - Circuit-specific corners for each measurement that are suitable for analog designs
- AFS AMS
 - Full-circuit verification including complex digital initialization sequence
 - Simple use model with the accuracy, and performance of AFS circuit simulator
 - Maintaining nanometer SPICE accuracy on blocks that were independently verified
- AFS Mega
 - Validate top-level array and signal chain at the transistor level, including parasitics
 - Verify long distance interaction between analog signal chains
 - Predict impact of IR drop across the array



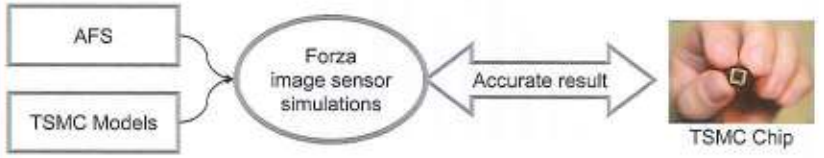
AFS in TSMC Custom Reference Flow



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Simulator and Foundry Model Accuracy

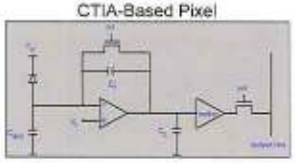
- The accuracy of the result of a simulation of a circuit is a function of
 - Simulator accuracy
 - Device model accuracy
- Simulator:
 - AFS delivers nanometer SPICE accuracy
 - AFS noise and jitter analysis based on BDA developed theory
 - Based on advanced stochastic nonlinear theory
 - Recognized as most accurate theory in industry today
- Device Models:
 - New first-order effects due to device noise require more accurate model parameter extraction
 - Device noise model parameters used in simulation from TSMC PDK



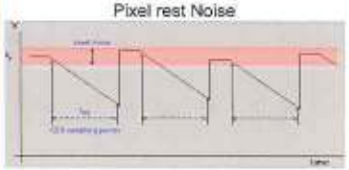
AFS TN: Pixel Reset Noise Characterization

- Caused by reset switch resistance thermal noise, amplifier thermal and 1/f noise
- Difficult simulation that requires transient noise analysis for accurate results

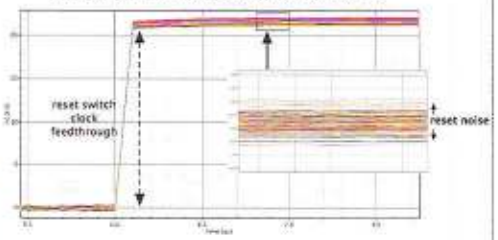
CTIA-Based Pixel



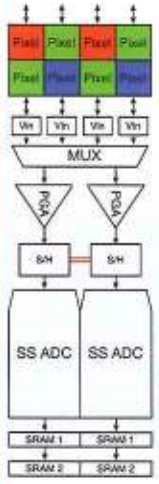
Pixel rest Noise



Reset noise from multiple transient noise sims



ACE: Analog Signal Chain Characterization



- Relies on AFS circuit simulator accuracy and performance
- Uses BDA's Analog Characterization Environment (ACE)

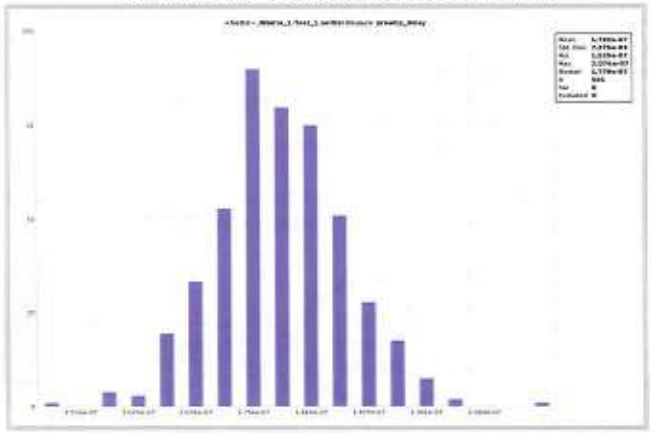
Transient response – PGA output



Simulator	Traditional SPICE	Parallel SPICE	AFS
Runtime	>60 min	15 min	1 min

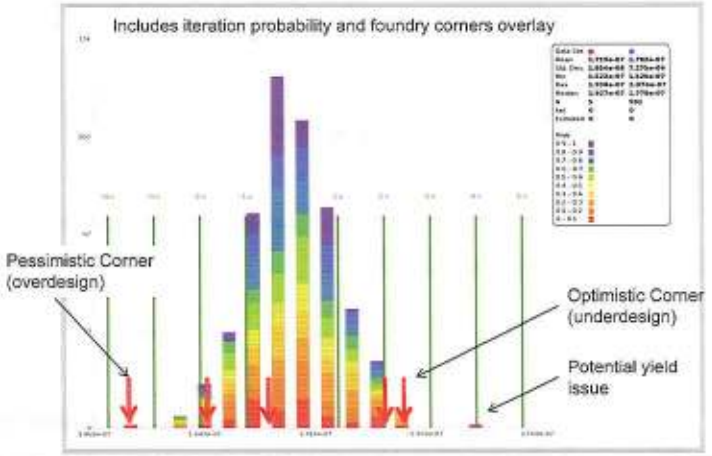
ACE: Analog Signal Chain Iteration Distribution

Preamp delay characterized in 500 MC runs



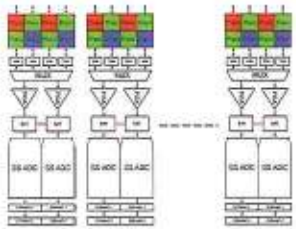
AFS Statistical Corners: Analog Signal Chain

Quickly target potential yield issues and create circuit-specific statistical corners

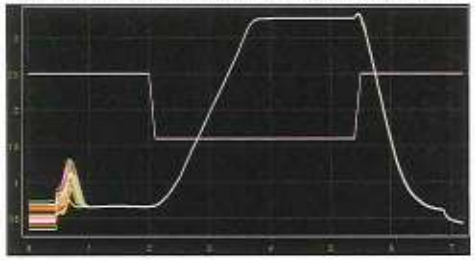


AFS Mega: Multiple Signal Chain Simulations

- Post-layout circuit simulation verifies analog signal chain signal variation
 - Verify signal variation due to IR drop, ground bounce and cross talk
 - SPICE-accurate simulation with ~29M elements and ~330K MOS devices
 - Simulation of 712 signal chains
 - AFS Mega Runtime: 21hs (to 7us sim time)
 - Simulation not possible with other SPICE-accurate simulators

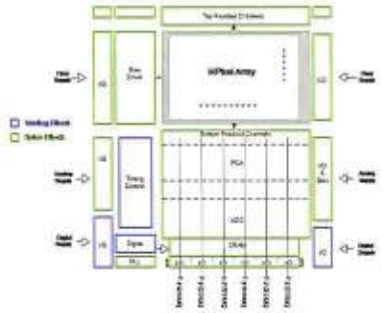


Transient response of multiple PGA output voltage signals

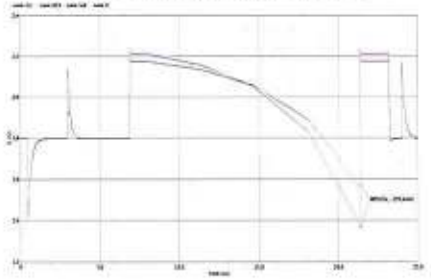


AFS AMS: Full-Circuit Verification

- Full chip response of a comparator preamp
- Modeled under various parasitic conditions
- AFS AMS speed and quick RTL changes allows high functional coverage



Preamp response to load vs. time



Conclusion

- The AFS Platform from Berkeley Design Automation has
 - Enabled Forza's efficient and accurate sign-off simulation methodology
 - Increased design productivity and reduced risk
- For High-Performance CMOS image sensor verification
 - Need AFS Transient Noise to validate pixel and analog signal chain noise
 - Need ACE and AFS Statistical to characterize the analog signal chain
 - AFS Mega enables pixel array and readout IR verification
 - AFS AMS delivers full-chip functional verification
- Forza Silicon's verification methodology provides
 - Accurate and efficient results
 - Intense characterization of pixel and analog signal chain
 - Accurate prediction of long distance interactions and IR drops
 - Tapeout confidence with full-chip functional verification

Design and Modeling Platform for the TSMC's FOWLP Reference Design Kit

Agilent

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

A FOWLP (Fan Out Wafer Level Packaging) flow has been enabled to show improved performance, low cost, and reduced size compared with other traditional package solutions.

The FOWLP architecture takes advantages of the package molding compound to integrate multiple chips within the same package. This FOWLP process starts with multiple dies placed on a carrier with molding compound. An ultra fine pitch Cu-PPI (Post Passivation Interconnect) is introduced to create inductors along with ball grid array connectors. The advantage of this technology is that an ultra-thin package can be achieved. In addition, it becomes possible to relocate on-chip inductors using Cu-PPI in package level, leading to smaller chip area and increasing Q factor of inductors.

It is noted that higher Q factor can effectively reduce power consumption and possess better thermal characteristics. This concept has been shown in TRx, PMIC and, PA modules and can be applied from 2D to 3D ICs. The overall FOWLP technology has been demonstrated in the HF RDK 5.0.

The paper describes the overall FOWLP flow and how Agilent EEsof solutions are enabled and qualified within the HF RDK 5.0. It goes from a front-to-back IPD (Integrated Passive Devices) design implementation, to dedicated RF circuit and EM simulation solutions for the multi-technology Wafer-level package integration of complete RF modules.

Design and Modeling Platform for the TSMC Fan Out Wafer Level Package (FOWLP) Reference Design Kit

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Che-Sheng Chen
Agilent Technologies




Feng-Wei Kuo
Tzu-Jin Yeh
Robert A. Mullen
Taiwan Semiconductor Manufacturing Company, Ltd.





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Outline

- RF design challenges
- TSMC – Agilent collaboration examples
 - Momentum qualification across process nodes
 - New 60-GHz Reference Design Kit (RDK) at 28nm and 65nm
 - IPD design enablement
- FOWLP (Fan Out Wafer Level Packaging) RDK
 - Technology overview
 - Correlation of EM & circuit simulation with measurements
 - Design flow and methodology
- Conclusion

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Time-to-Market – Today's Tablets As an Example

Data
Wi-Fi® 802.11a/b/g/n
possible: 802.11ac

Location
A-GPS
possible: Galileo, Beidou, GLONASS

Personal Connectivity
Bluetooth v4.0
possible: 802.11ad/WiGig



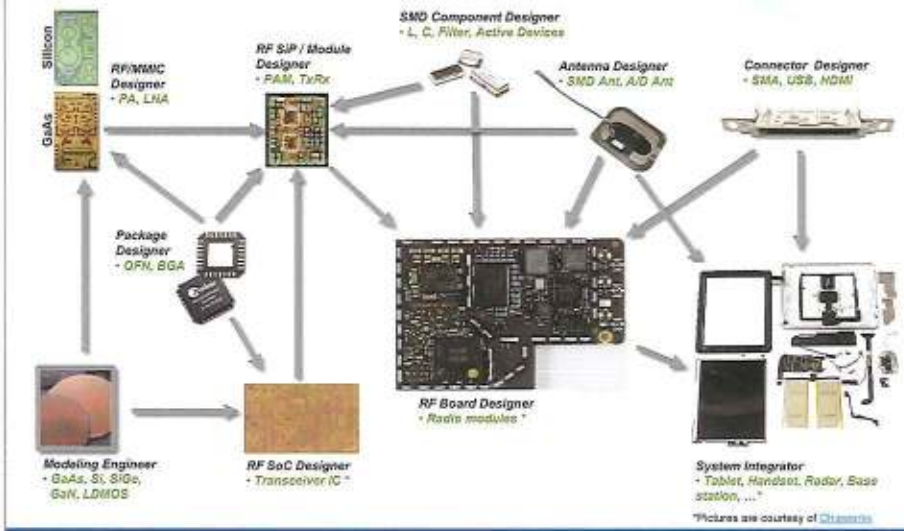
Communications
4G LTE
Also: LTE-Advanced, MIMO

HSPA, HSPA+
DC-HSDPA
Also: GSM/EDGE, WCDMA, Multi-Standard Radio (MSR)

- Increasing integration with multiple complex systems placed in close proximity
 - Increasing design complexity and compaction
 - Concurrent design teams across companies
 - Verification across design domains (IC/package/board)

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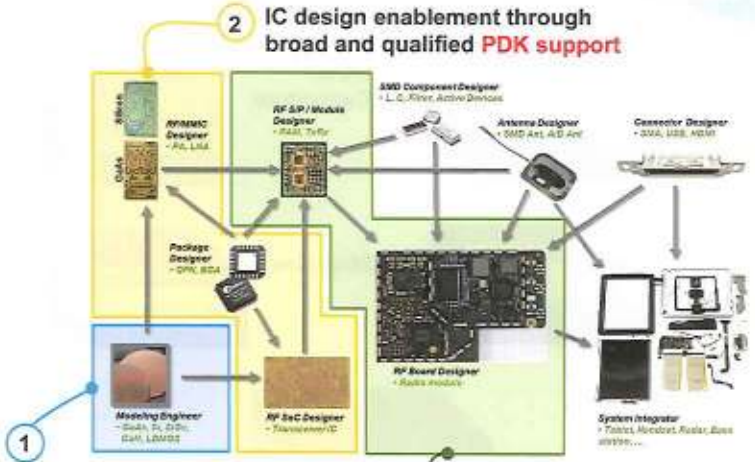
Components and Design Tasks Toward a System



*Pictures are courtesy of Qualcomm

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TSMC – Agilent Collaborations: Three Main Areas



*Pictures are courtesy of Chipworks

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Momentum Qualified Across TSMC Processes

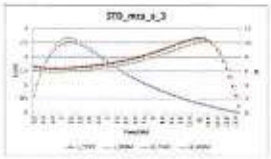
Momentum qualified for TSMC's 90, 65, and 40nm processes

- Momentum passed TSMC qualification tests against measurements up to 30 GHz for different configurations
- +20 inductors on average validated with different metal stacks for symmetric, un-symmetric and center-tapped inductors configurations

Available for download at TSMC online

Qualified EM Tools

Technology Node	Vendor	EM Tool Name	Tool Ver.	Qualification Report(link)
40nm	Agilent Technologies	Momentum	Pls refer to EM Qual Report	Y (Download)



Sample results for 40 nm

Additional Momentum Modules and ADS PDKs available

- +50 Momentum modules available for TSMC processes down to 28 nm
- ~20 ADS front-end PDKs available for TSMC processes
- Full front-to-back ADS for TSMC Integrated Passive Device (IPD) process

For further details go to

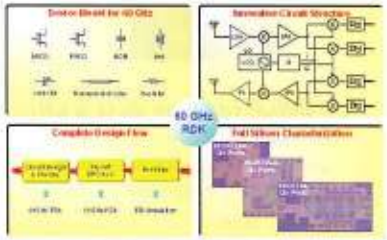
http://www.agilent.com/find/eesof-partners-tsmc

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TSMC – Agilent Collaboration: Two IC Enablement Examples

60GHz RDK for 65nm & 28nm

- RF frontend circuits (LNA, PA, and VCO)
- Achieve reliable measurement results
- Enable RF top-down design methodology to perform system level simulation with behavior model solution
- Extra devices/ transmission line support



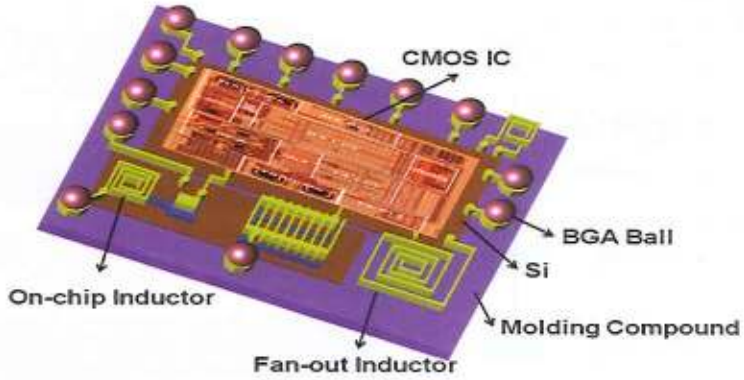
IPD design dnablement

- Integrated Passives Devices process for the production of baluns, filters, couplers, and diplexers on a separate die
- Used in RF modules & RF system-in-packages in portable, wireless and RF applications
- Provide complete ADS front-to-back PDK



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FOWLP Technology Overview



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FOWLP Opportunities

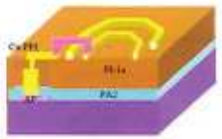
- Today's transceivers must have good performance and a smaller form factor and longer battery life
- A SiP-like approach called **Fan-Out Wafer Level Package (FOWLP)** technology benefits circuit performance and lowers the power
- **FOWLP** can be used for MEMS, Bluetooth, GPS, Audio, Power Management, IC controller, and PA modules
- **FOWLP** uses plastic package technology with its copper PPI (Post Passivation Interconnect) layers to form high efficient inductors, capacitors, and T-line devices that allow these components to step off-chip
- **FOWLP** combines design solution between chip and package for better specs, smaller form factor, and lower costs



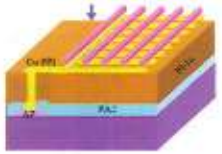
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FOWLP Available Passive Devices
with thick metal and low substrate losses

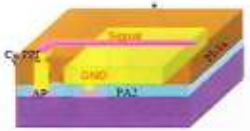
Inductors
Transformers
Baluns



MOM
Capacitors



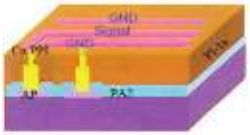
Microstrip
Lines



Strip Lines



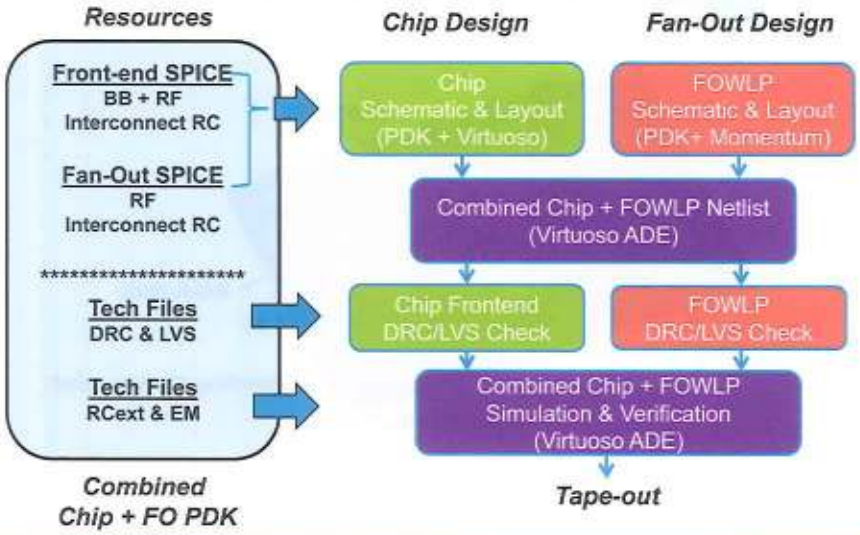
CPW
(Co-planer Waveguides)



*TSMC Illustrations

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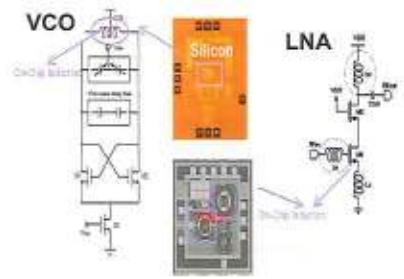
TSMC FOWLP Co-Design Flow



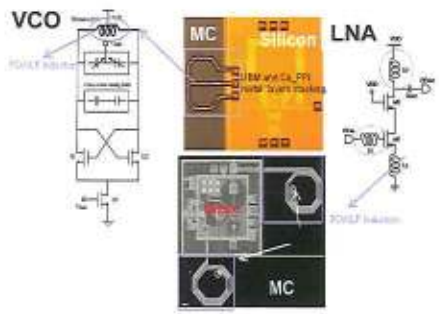
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Single Chip 65nm Inductor Vs. FOWLP Inductor

Single Chip



FOWLP

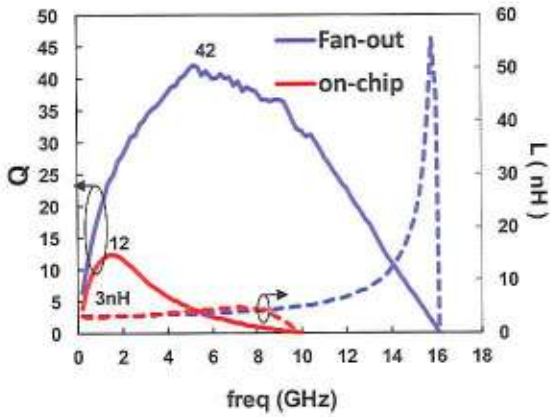


Single chip 65nm VCO & LNA
Larger chip area
Higher current
Lower RF performance
Higher cost

FOWLP w/ 65nm VCO & LNA
Smaller chip area
Lower current consumption
Better RF performance
Lower costs

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Comparing FOWLP to On-chip Inductors



VCO FOWLP Performance Improvement

Parameter	Single Chip 65nm CMOS	Pwr Opt	FOWLP with 65nm CMOS	FOWLP Improvement
Supply Voltage	1.2		1.2	
Frequency Range (GHz)	4.5 – 5.8		4.4 – 5.7	
Phase Noise (dBc/Hz @1MHz)	-119.5	hi	-130	8.8%
		lo	-120	4.2%
FOM (dBc/Hz)	-183.5	hi	-195.5	6.5%
		lo	-186.7	1.7%
Power (mW)	10.7	hi	9.0	15.9%
		lo	3.6	66.4%

FOWLP area reduction ~20%

LNA FOWLP Performance Improvement

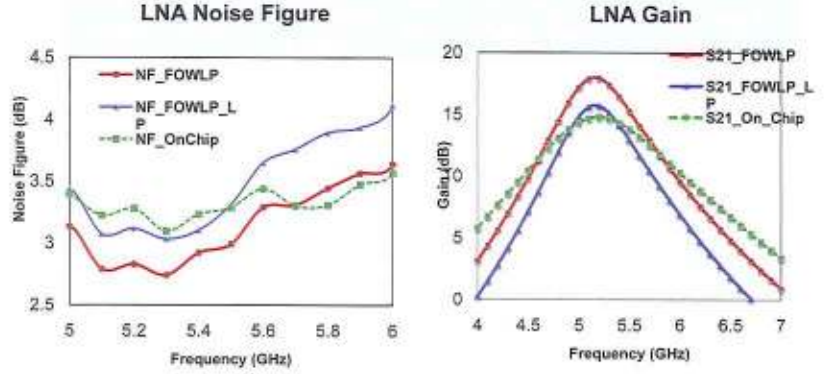
Parameter	Single Chip 65nm CMOS	Pwr Opt	FOWLP with 65nm CMOS	FOWLP Improvement
Supply Voltage	1.2		1.2	
Frequency Range (GHz)	5.2		5.2	
Gain (dB)	15.0	hi	18.0	20.0%
		lo	15.8	5.3%
NF (dB)	3.3	hi	2.7	17.7%
		lo	3.1	6.9%
Power (mW)	4.8	hi	4.5	6.3%
		lo	2.4	50.0%

FOWLP area reduction ~50%

Overall Receiver Performance Comparisons

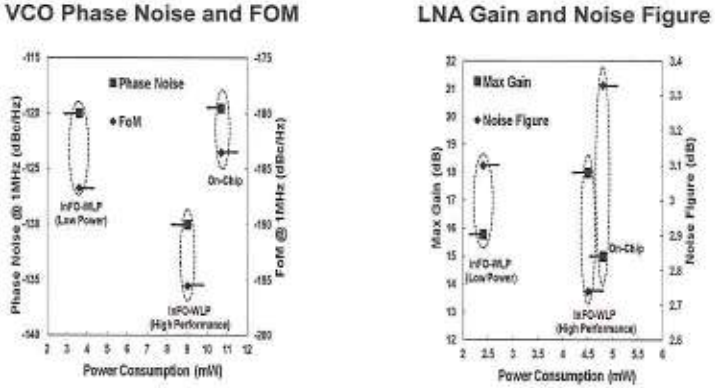
	ISSCC 2007	ISSCC 2010	ISSCC 2012	FOWLP Example	Units
Technology	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS + FOWLP	
Supply Voltage	1.5	1.2	1.35	1.2	V
Frequency	5	4.8 – 5.9	6	5.2	GHz
Phase Noise	-115	-114	-123	-129	dBc/Hz @1MHz
Receiver Noise Figure	4	6	4	3	dB
Receiver Sensitivity at 54Mb/s	-74	-76	-76	-77	dBm
Current	49	81	93	~50	mA

Measured LNA FOLWP Vs. On-Chip Results



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Measured Performance VCO & LNA Advantages

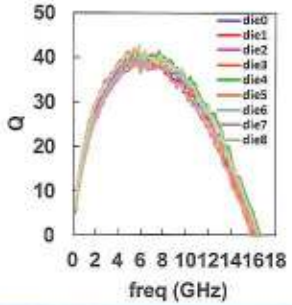


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FOWLP Process Stability
Example: Inductor Uniformity

For uniformity of the L=3.4nH inductor:

- Peak Q factor: 3.28%
- Self-resonance freq.: 1.68%
- Inductance: 0.35%



Category	Q peak	fsr [GHz]	L (nH)
Max	42.61	16.60	3.41
Min	38.76	15.80	3.37
Median	40.40	16.20	3.40
Uniformity	3.28%	1.68%	0.35%

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FOWLP Process Summary

- FOWLP approach has been shown to be more effective than a single chip solution
- FOWLP technology Is a comprehensive solution that renders a smaller form factor, better electrical and thermal performance, increased density, reduced costs, and more flexibility than a single chip solution
- TSMC has demonstrated that high quality passive components can be embedded into a FOWLP substrate and coupled with CMOS circuit blocks with good circuit performance and power reduction
- A prototype SiP integrated RF receiver module was built with commercial bare-die components to demonstrate the feasibility
- This technology is suitable for RF circuits that employ high Q inductors and capacitors such as LNAs and VCOs

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FOWLP Design Flow – Agilent EEsof Collaboration

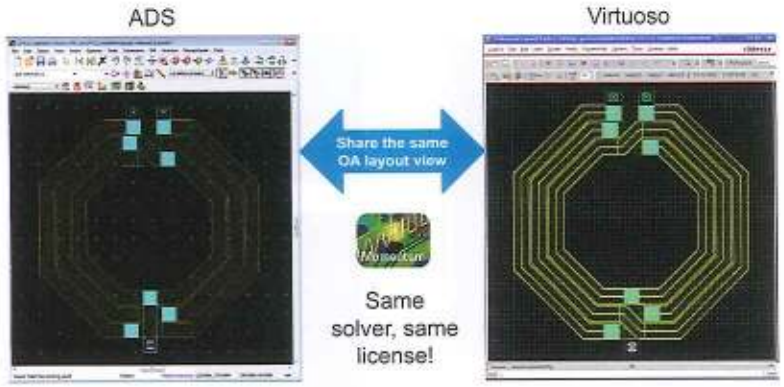
FOWLP RDK collaboration goals

- Prove correlation of EM & circuit simulations with measurements
- Provide a design flow that enables a true co-design across boundaries

1. Prove Momentum EM simulation correlation against measurements for individual FOWLP embedded passives
2. Circuit simulation of LNA (& VCO) in GoldenGate and compare against measurements
3. Simulate full LNA (& VCO) fan-out WLP layout with FEM
 → Investigate impact of multi-technology (silicon & molding) nature of carrier
4. Add solder balls and mount onto PCB test board
 → Investigate impact of solder balls, RDL routes, board traces, … on VCO (&LNA) performances

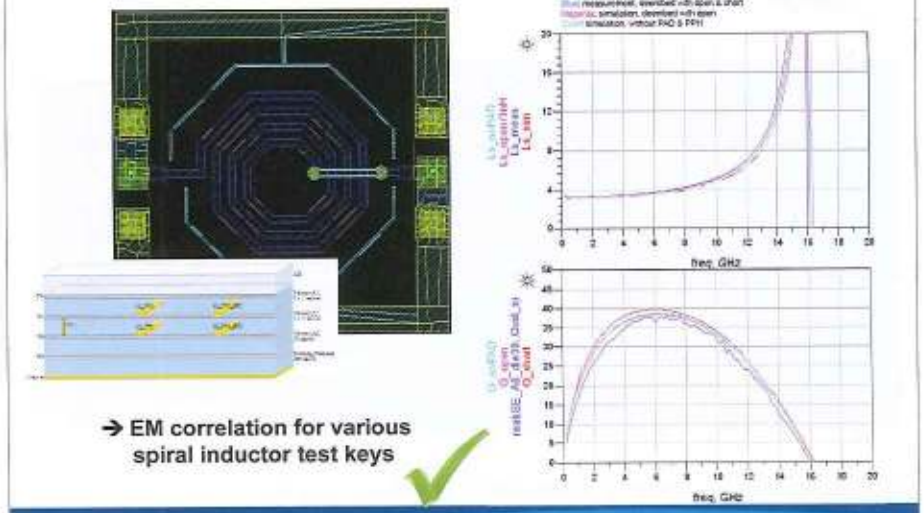
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Interoperable Flow for On-Chip and FOWLP Passive Component Design Across Virtuoso & ADS



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FOWLP Embedded Passives Correlation

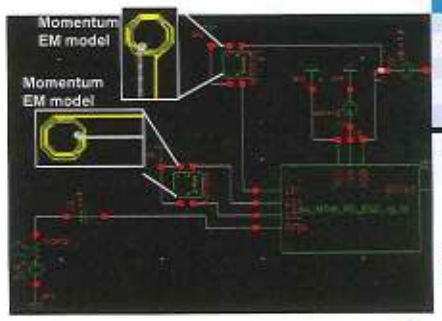


→ EM correlation for various spiral inductor test keys

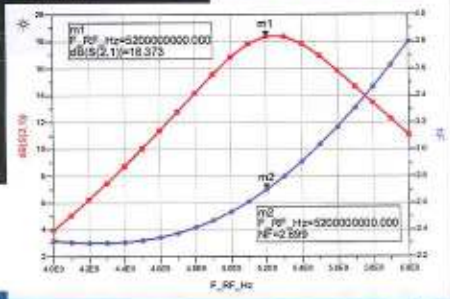
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Circuit Simulation of LNA in GoldenGate and Compare Against Measurement

LNA test bench:



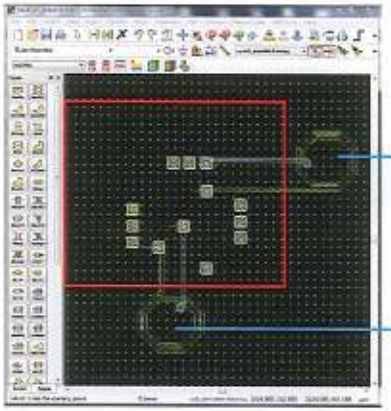
Parameter	Pwr Opt	FOWLP measurement	FOWLP GG simulation	Sim vs. measurement
Supply Voltage		1.2	1.2	
Frequency (GHz)		5.2	5.2	
Gain (dB)	hi	18.0	18.3	1.7%
NF (dB)	hi	2.7	2.7	0%
Power (mW)	hi	4.5	4.8	6.7%



→ Circuit simulations correlate for key measurements

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FOWLP Design and Modeling Platform



Individual spiral structures

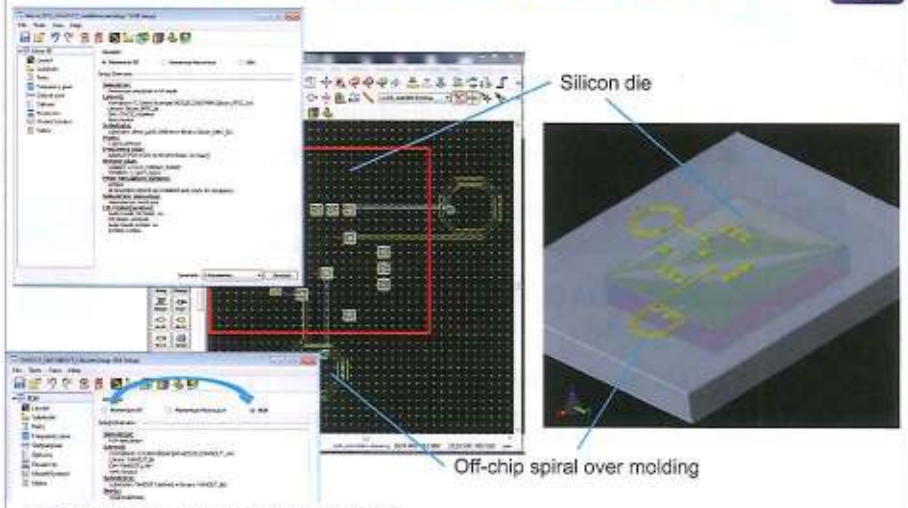




➔ Spirals and interconnects simulated over molding only

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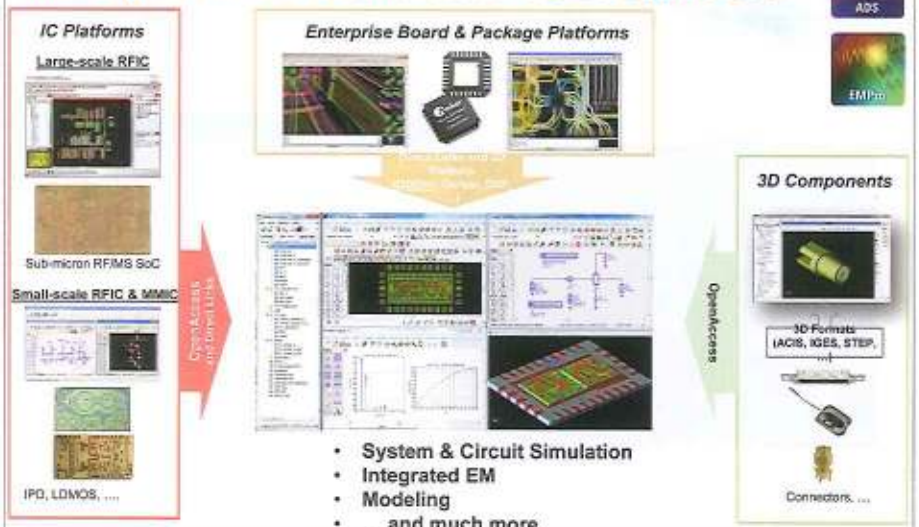
ADS Enables Multi-technology Co-design



➔ **Switch from Momentum to FEM!**

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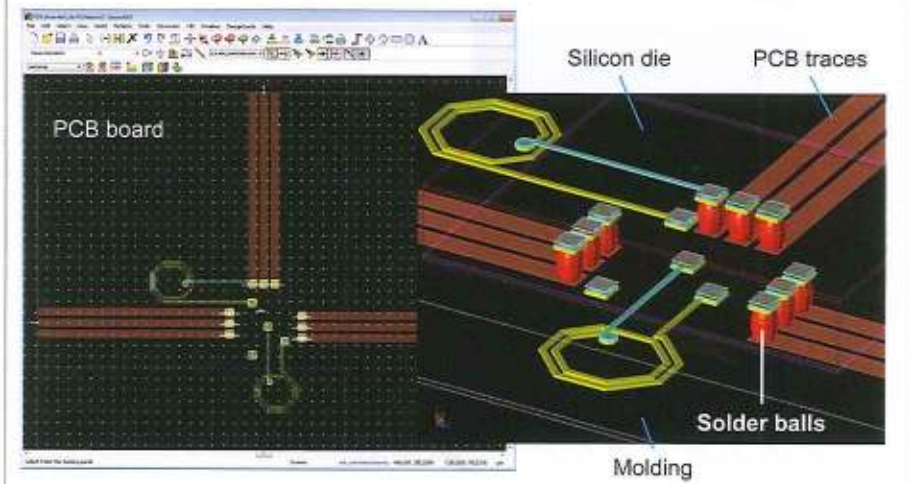
Interoperable RF Module/SiP Co-Design Flow



- **System & Circuit Simulation**
- **Integrated EM**
- **Modeling**
- **... and much more**

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Expand FOWLP Configuration to Full System



➔ **Enables true co-design & optimization of complete system**

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Conclusion

- A close collaboration between TSMC and an EDA partner ensured silicon accurate results at advanced process nodes
- TSMC and Agilent EEsof have collaborated over the years on multiple high frequency projects -- most recently
 - 60GHz demonstrating extreme complex design with 28nm chips
 - Integrated Passive Devices (IPD)
 - FOWLP technology development with 65nm chips
- Improved performance and smaller form factor translating single chip RF front-ends into a FOWLP topology
- Collaboration extends beyond design domains to leverage the best technology from both sides

More details at: http://www.agilent.com/find/eesof-partners-tsmc

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Case Study of 28nm Option Selection for Wireless Baseband Co-processor

IMEC

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ABSTRACT

The transition of products from the 40nm node to 28nm has brought with it an unprecedented increase in number of technology options to choose from. This presentation provides a case study of how the technology selection (for example, gate length offsets, threshold voltages, supply voltages, ...) for a 28nm wireless baseband co-processor was optimized. Our goal was to minimize total (static+dynamic) power dissipation while maintaining the throughput constraints of the IEEE 802.11ad (WiGig) standard as a function of the number of selected co-processor cores. In this study both HP and HPM flavors were studied, and for each of these multiple threshold voltages, gate- length offsets, supply voltages and cell track heights were assessed.

The assessment of such a large number of options was enabled by the use of a unique method called trace analysis. This procedure takes the passive timing and power reports from a synthesized and timed reference option and converts them into active functions called traces, which can take additional libraries for other flavors and options as input arguments. Traces can re-calculate timing and power results in seconds with a benchmarked accuracy of approximately 1%. By means of this method we populated a clock rate versus power graph with the predicted performance of the co-processor implemented with over 30 options using library timing and power reports of a 28nm HPM worst-case 9-track reference. Our analysis method used libraries characterized at slow corners to calculate critical path clock rates and typical corners for the calculation of power. Overlaid on this plot were the contours of the throughput required by the IEEE 802.11ad standard and contours for energy efficiency, expressed as pJ/bit. This enabled us to locate the potential technology options that would satisfy an increasingly severe set of performance constraints as a function of the number of processor cores selected. The optimum technology option selection was observed to depend on the number of cores selected, and several of these were not considered as potential low-power technology option solutions prior to the start of the study.

Case study of 28nm option selection for wireless baseband co-processor

Paul Zuber, †Peter Debacker, Ilse Vos , †Veerle Derudder, †Frederik Naessens, †Antoine Dejonghe, Phillip Christie

imec services
†imec Green Radio program

imec

OVERVIEW

- imec services and imec Green Radio program
- Low Density Parity Checking (LDPC) core and the 60 GHz IEEE 802.11ad WiGig standard
- Rapid technology assessment of LDPC core using timing and power traces
- TSMC 28nm technology targeting results for
 - Multi-core LDPC single Vt implementations
 - Multi-core LDPC multi-Vt implementations
- Summary

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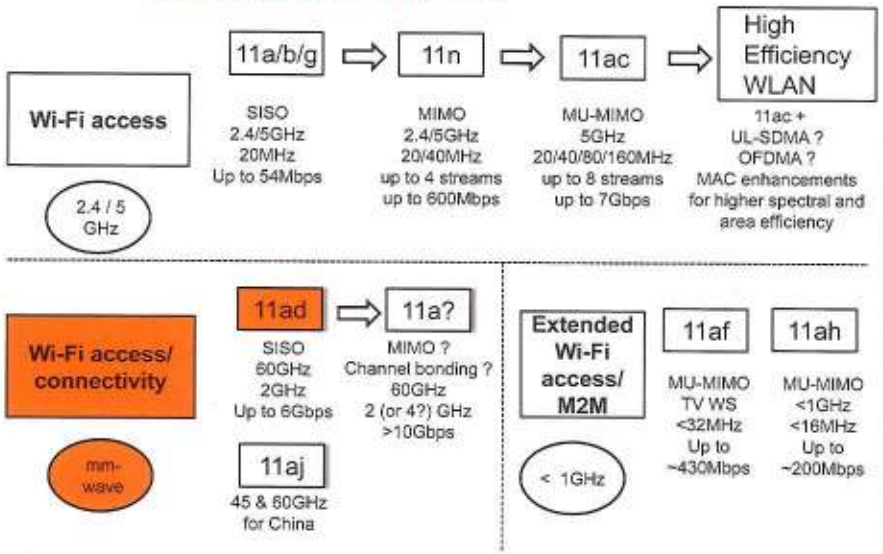


imec SERVICES AT GLANCE

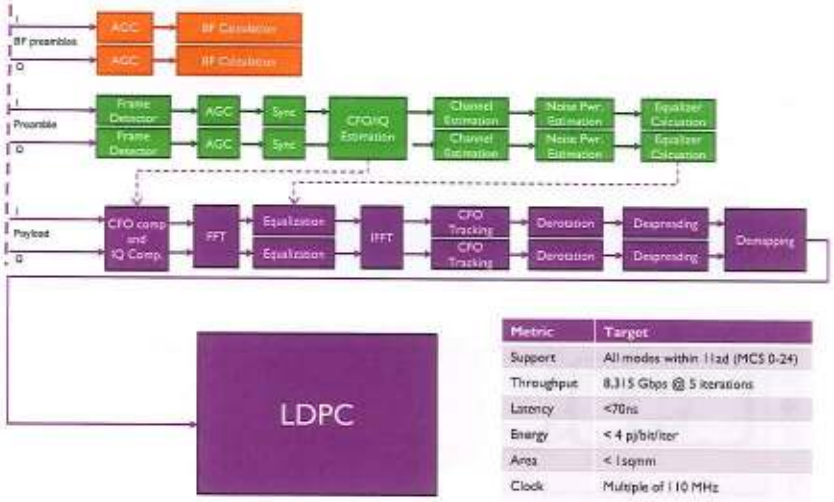




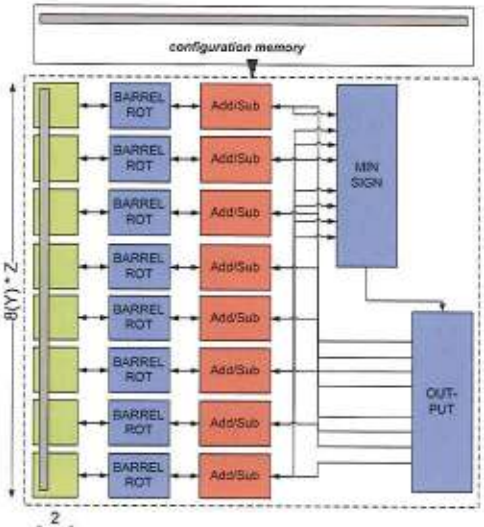
THE 802.11 FAMILY



LOW DENSITY PARITY CHECK (LDPC) KEY COMPONENT OF 802.11ad STANDARD



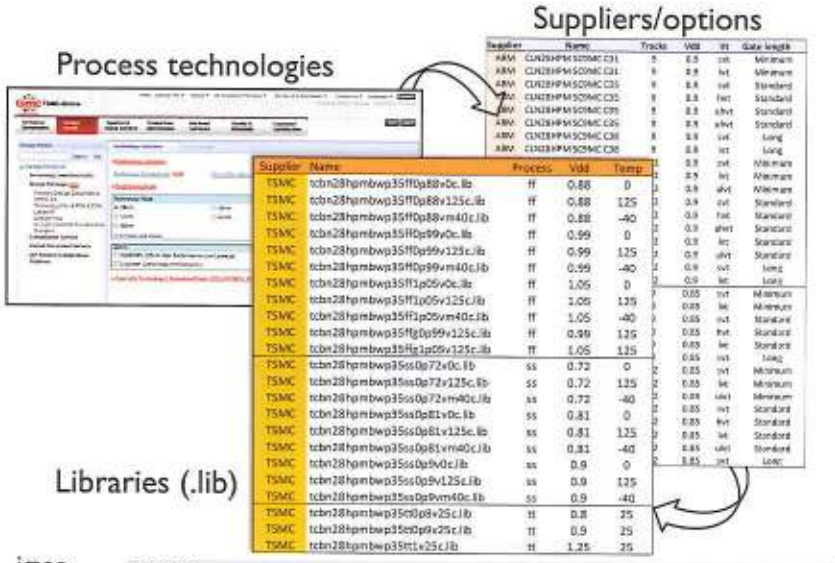
IMEC'S BLOX-LDPC ASIP CORE CAN MEET THESE EXTREMELY CHALLENGING SPECS



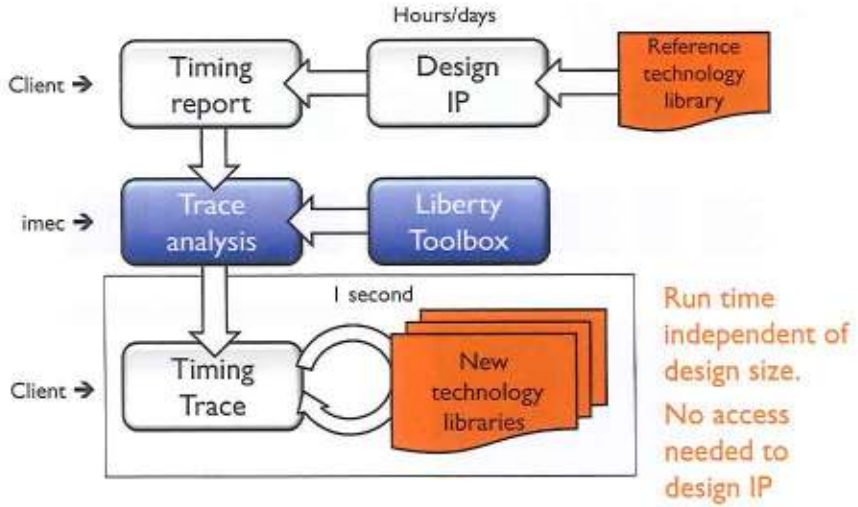
TARGET
THE ASIP COMPANY

MOBILE WORLD CONGRESS
Barcelona | 25 – 28 February 2013

TSMC TECHNOLOGY CHOICES



TIMING TRACES

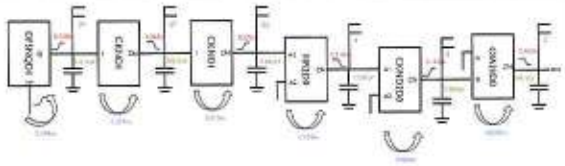


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TIMING REPORT

Cadence RTL Compiler

```
DATA_PATH
  Cell(Instance)  Cell(Type)  Fanout  Load  Slew  Delay  Arrival
  ------------------------------------------------------------
  INST (/atomic_exp) (CP) (^) (Q) (^) () (DFSNQD1) (0.248) (0.000) (0.338) () (0.248) (3.638) () (23) ()
  NET () () () () () () (/ctl_dwt_atomic_q) () (0.000) (0.000) (0.226) (0.054) (0.248) (3.638) () () ()
  INST (/u_dec/g1793) (I) (^) (ZN) (v) () (CKND1) (0.218) (0.000) (0.267) () (0.468) (3.858) () (27) ()
  NET () () () () () () (/u_dec/net_2362) () (0.000) (0.000) (0.267) (0.050) (0.468) (3.858) () () ()
  INST (/u_dec/g22024) (I) (v) (ZN) (^) () (CKND1) (0.210) (0.000) (0.272) () (0.678) (4.068) () (23) ()
  NET () () () () () () (/u_dec/n_79) () (0.000) (0.000) (0.272) (0.042) (0.678) (4.068) () () ()
  INST (/u_dec/g21894) (A1) (^) (ZN) (v) () (NR2D2) (0.074) (0.000) (0.110) () (0.752) (4.142) () (4) ()
  NET () () () () () () (/u_dec/n_194) () (0.000) (0.000) (0.110) (0.207) (0.752) (4.142) () () ()
  INST (/u_dec/g21715) (A1) (v) (ZN) (^) () (CKND2D0) (0.060) (0.000) (0.115) () (0.812) (4.202) () (2) ()
  NET () () () () () () (/u_dec/n_340) () (0.000) (0.000) (0.115) (0.504) (0.812) (4.202) () () ()
  INST (/u_dec/g21550) (B) (^) (ZN) (v) () (OAI21D0) (0.098) (0.000) (0.168) () (0.910) (4.300) () (5) ()
  NET () () () () () () (/u_dec/n_1216) () (0.000) (0.000) (0.168) (0.010) (0.910) (4.300) () () ()
  ...
END_DATA_PATH
```



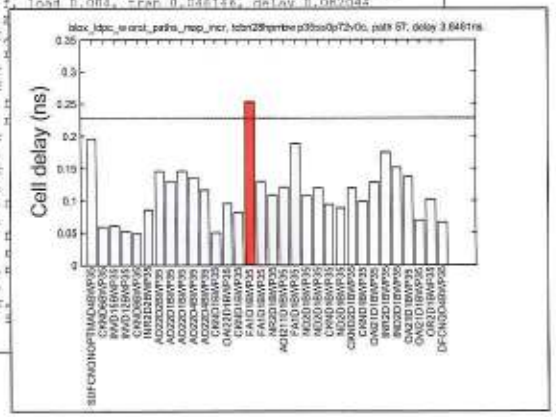
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TIMING TRACE

Unix command line program

```
>> blox_ldpc_worst_paths_map_incr tcbn28hpmbwp35ss0p72v0c.lib --verbose

path 1
  DFCNQOPTMAD8BWP35: CP ,r ,Q, f, load 0.004, tran 0.029127, delay 0.17338
  IND2D4BWP35: A1 ,f ,ZN, f, load 0.004, tran 0.046146, delay 0.082044
  NR2OPTPAD2BWP35: A1 ,f ,
  NR2D3BWP35: A1 ,r ,ZN, f,
  NR2XD2BWP35: A2 ,f ,ZN, r
  AOI21OPTPBD4BWP35: A1 ,r
  OAI21OPTPBD2BWP35: A1 ,f
  ND2XD3BWP35: A2 ,r ,ZN, f
  MUX2ND1BWP35: S ,f ,ZN, r
  OAI21OPTPBD1BWP35: A2 ,r
  TPNR2D3BWP35: A1 ,f ,ZN,
  AOI21OPTPBD6BWP35: A1 ,r
  TPND2D2BWP35: A1 ,f ,ZN,
  OAI21OPTREPBD4BWP35: B ,r
  CKND3BWP35: I ,f ,ZN, r,
  INR2D2BWP35: B1 ,r ,ZN, f
  IAO21D2BWP35: B ,f ,ZN, r
  OAI21OPTRESBD4BWP35: B ,r
  CKND1BWP35: I ,f ,ZN, r,
  OA33D1BWP35: B3 ,r ,Z, r,
  OAI21D2BWP35: B ,r ,ZN, f
  ...
```



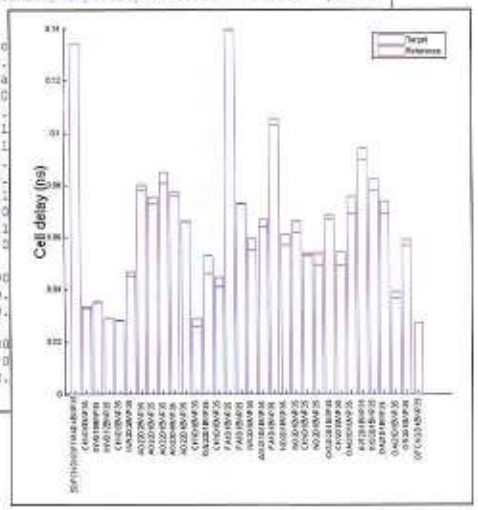
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TRACE BENCHMARKING

Differential timing plot with reference library

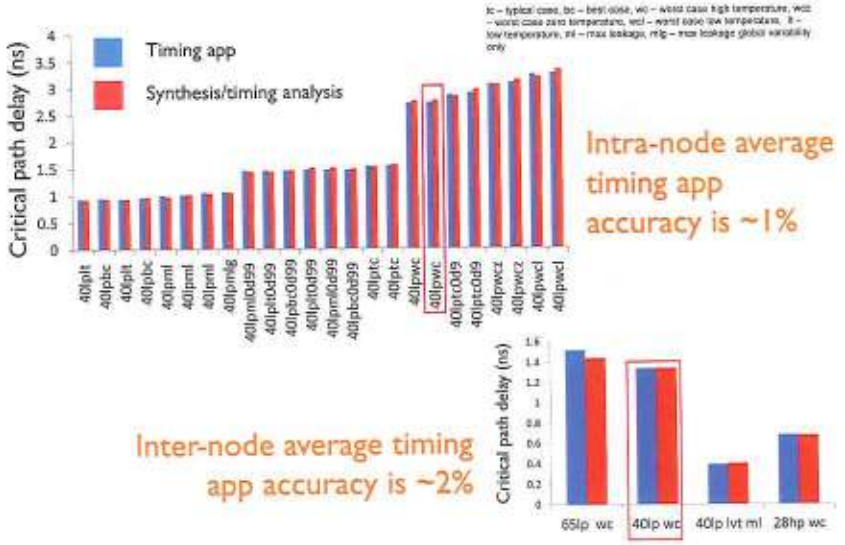
```
>> blox_ldpc_worst_paths_map_incr tcbn28hpmbwp35ss0p81v0c.lib --verbose --plot 2

path 1
  DFCNQOPTMAD8BWP35: CP ,r ,Q, f, lo
  IND2D4BWP35: A1 ,f ,ZN, f, load 0.
  NR2OPTPAD2BWP35: A1 ,f ,ZN, r, loa
  NR2D3BWP35: A1 ,r ,ZN, f, load 0.0
  NR2XD2BWP35: A2 ,f ,ZN, r, load 0.
  AOI21OPTPBD4BWP35: A1 ,r ,ZN, f, l
  OAI21OPTPBD2BWP35: A1 ,f ,ZN, r, l
  ND2XD3BWP35: A2 ,r ,ZN, f, load 0.
  MUX2ND1BWP35: S ,f ,ZN, r, load 0.
  OAI21OPTPBD1BWP35: A2 ,r ,ZN, f, l
  TPNR2D3BWP35: A1 ,f ,ZN, r, load 0
  AOI21OPTPBD6BWP35: A1 ,r ,ZN, f, l
  TPND2D2BWP35: A1 ,f ,ZN, r, load 0
  OAI21OPTREPBD4BWP35: B ,r ,ZN, f,
  CKND3BWP35: I ,f ,ZN, r, load 0.00
  INR2D2BWP35: B1 ,r ,ZN, f, load 0.
  IAO21D2BWP35: B ,f ,ZN, r, load 0.
  OAI21OPTRESBD4BWP35: B ,r ,ZN, f,
  CKND1BWP35: I ,f ,ZN, r, load 0.00
  OA33D1BWP35: B3 ,r ,Z, r, load 0.0
  OAI21D2BWP35: B ,r ,ZN, f, load 0.
  ...
```

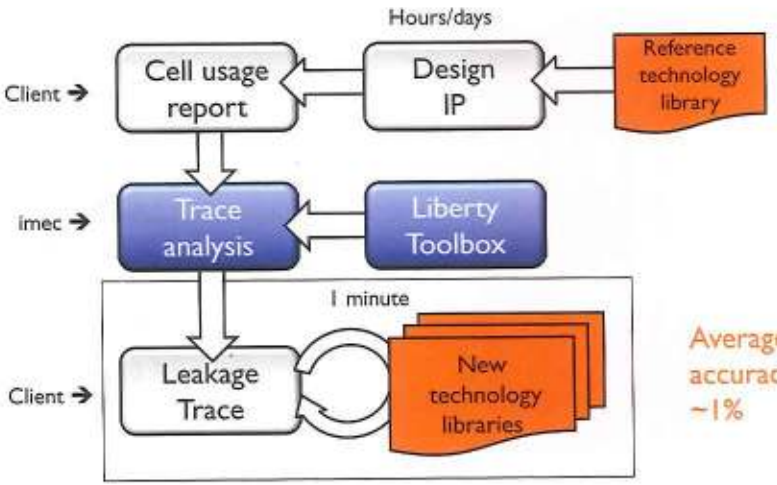


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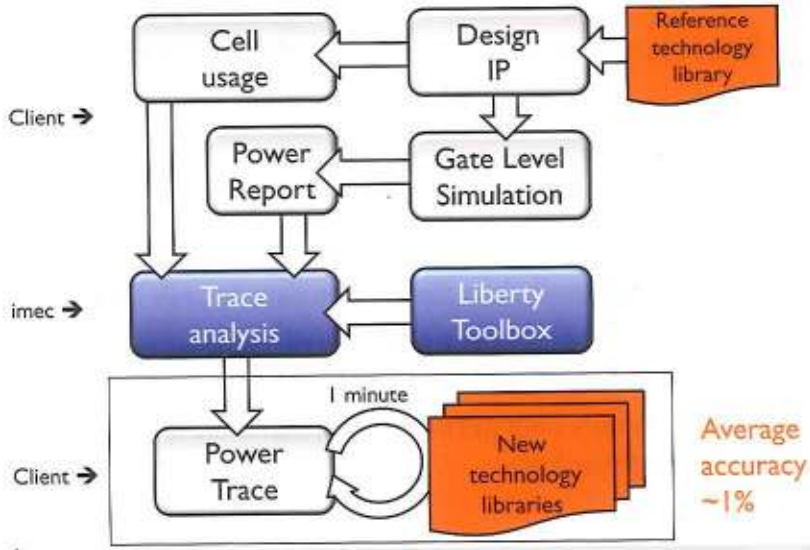
BENCHMARKING



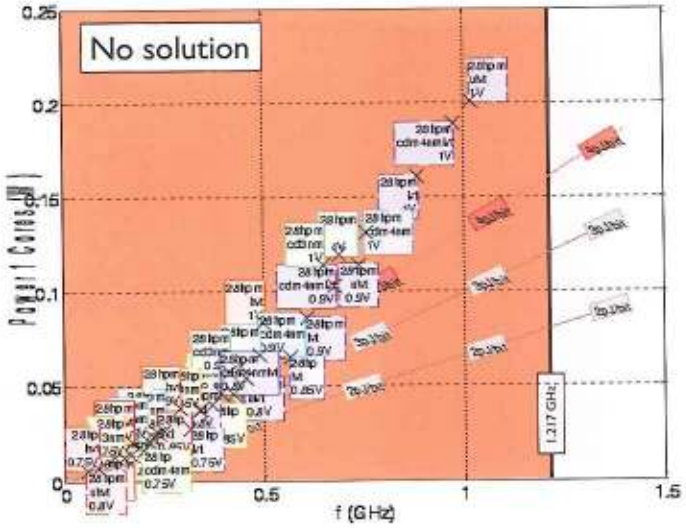
LEAKAGE TRACE GENERATION



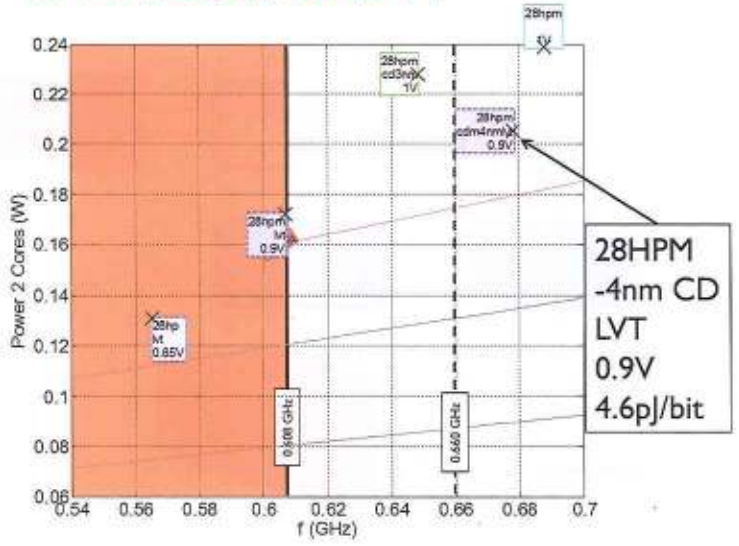
DYNAMIC POWER TRACE GENERATION



1 CORE, SINGLE VT

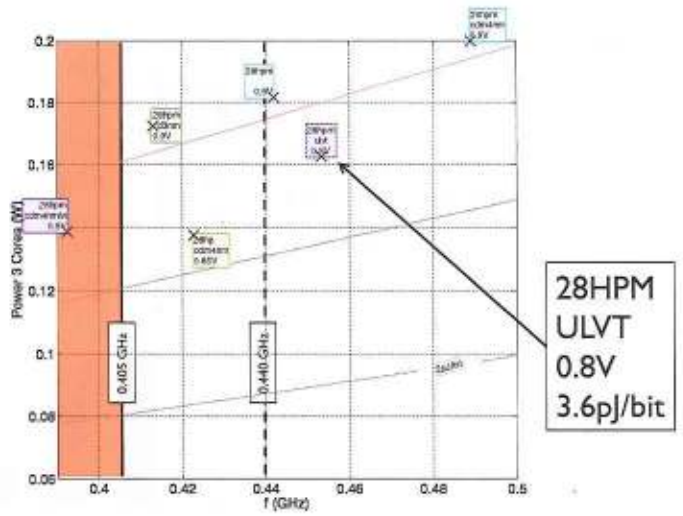


2 CORES, SINGLE VT



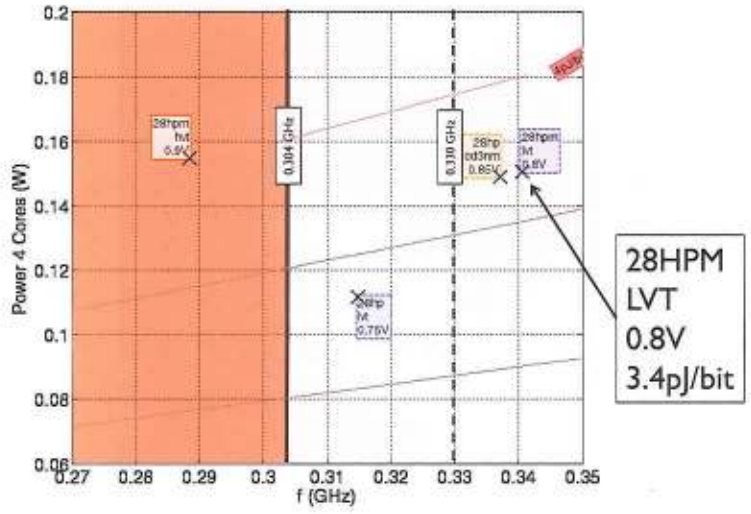
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3 CORES, SINGLE VT



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4 CORES, SINGLE VT



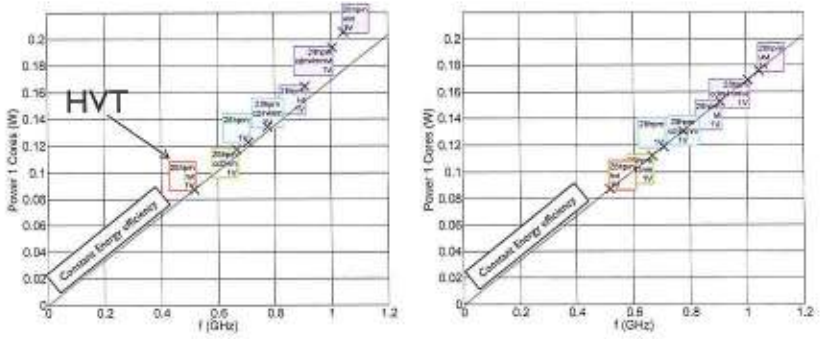
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MULTI-VT IMPLEMENTATION

- Separate traces calculate critical path delay and power
- Emulates high threshold voltage cell insertion in non-critical paths
- Approach assumes that critical path cells are a small proportion of the total
- The results recalculate the power data for HVT cells but retain the previously determined options for critical path delay.
- HVT insertion only performed for libraries at the same supply voltage

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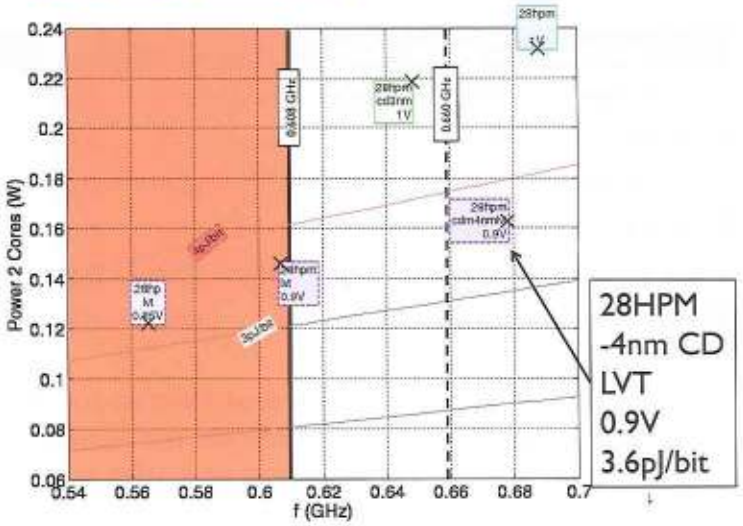
MULTI-VT IMPLEMENTATION



The effect of using HVT cells in power traces is to translate the data points onto the energy efficiency contour of the HVT data point

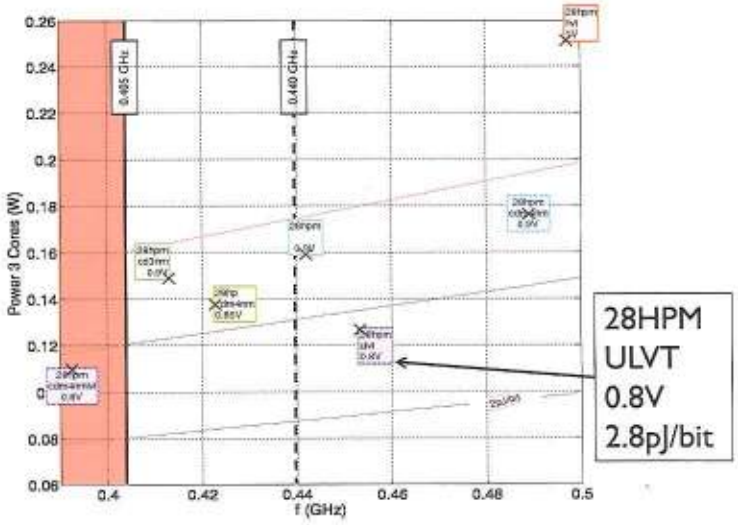
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2 CORES, MULTI-VT



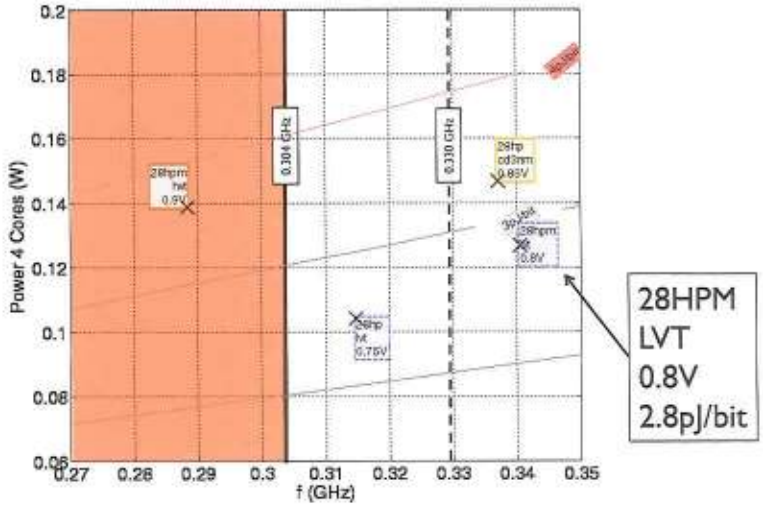
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3 CORES, MULTI-VT



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4 CORES, MULTI-VT



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TECHNOLOGY TARGETING RESULTS

Configuration		Option	Clk	CD	VT	Vdd	PJ/bit
2 core	Single Vt	HPM	660	-4nm	LVT	0.9V	4.6
	Multi Vt	HPM	660	-4nm	LVT	0.9V	3.6
3 core	Single Vt	HPM	440	0	ULVT	0.8V	3.6
	Multi Vt	HPM	440	0	ULVT	0.8V	2.8
4 core	Single Vt	HPM	330	0	LVT	0.8V	3.4
	Multi Vt	HPM	330	0	LVT	0.8V	2.8

- Optimal technology option is dependent on number of cores
- More cores are more energy efficient but require larger area
- Multi-Vt option has bigger impact on smaller number of cores

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SUMMARY

- 28nm implementation of IEEE 60GHz 811.ad WiGig standard requires careful technology assessment to achieve required power and performance specifications
- Collaboration between imec services and imec Green Radio program to select best technology for LDPC core
- Timing and power traces generated from a reference design were used to rapidly assess the speed and energy efficiency of 60 different 28nm HP and HPM technology options.
- Both single and multi-Vt strategies were applied to different numbers of LDPC cores.
- The most energy efficient implementation used three cores with 0.8 V HPM ULVT/HVT libraries at 440 MHz using 2.8pJ/bit.

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NOTE

Synopsys Laker Custom Layout and Calibre Interfaces: Putting Calibre Confidence in Your Custom Design Flow

Mentor Graphics

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ABSTRACT

While every design must pass sign-off before going to the foundry, it is inefficient to wait until the very end of the design process to run the sign-off checks. For this reason, Calibre provides interfaces to both custom and digital design tools which enable engineers to check against the sign-off decks throughout the design process. Through close cooperation between Mentor and Synopsys, Synopsys Laker users can check with Calibre "on the fly" during design to speed creation of design-rule correct layout, including electrically-aware voltage-dependent DRC checks.



Synopsys Laker Custom Layout and Calibre Interfaces:

Putting Calibre Confidence in Your Custom Design Flow

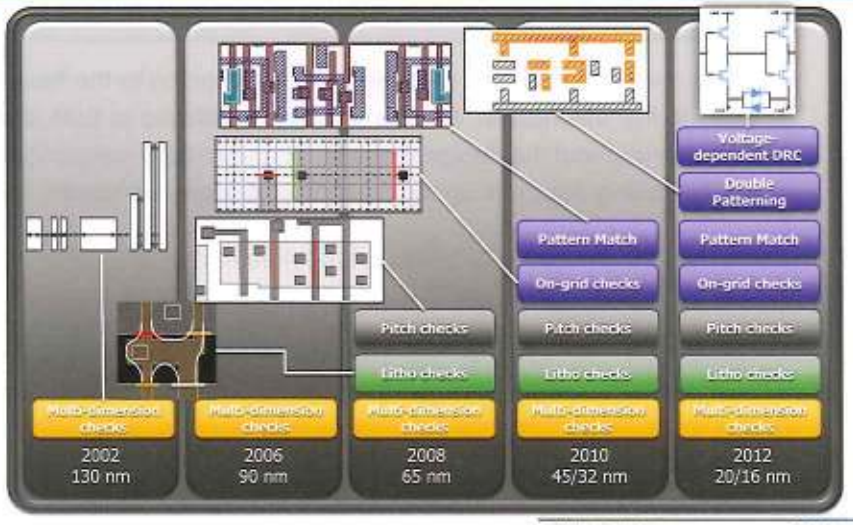
Joseph C. Davis

Product Marketing Director, Calibre Interfaces

Mentor Graphics

Mentor Graphics

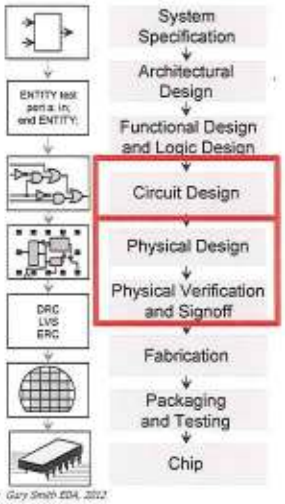
Physical Verification Trends: Increasing DRC Complexity



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Design Flow Is Changing



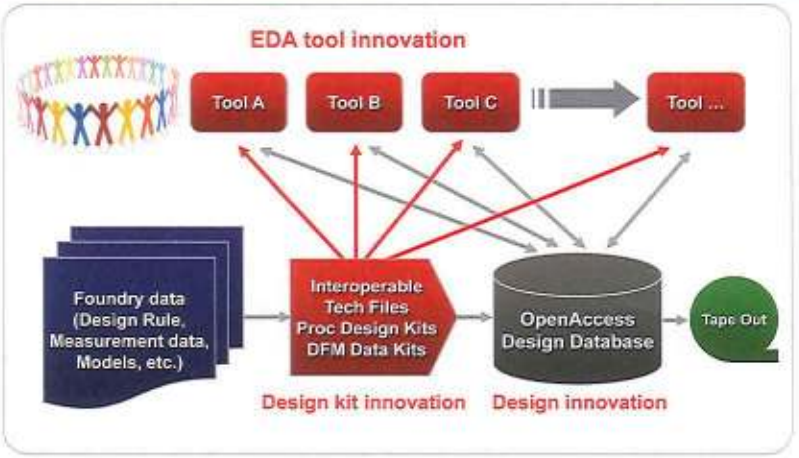
Source: Gary Smith EDA, 2012

- IC design flow has always attempted to be modular
- Since 90nm, the ability to separate electrical design from physical design and verification has been eroding
- DRC's are introduced in an attempt to ensure as much independence between electrical and physical domains, but is not always sufficient

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Interoperability Drive

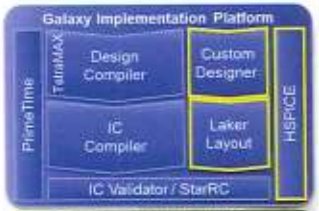


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Synopsys Comprehensive Custom & AMS Solution

Integrated Analog and Digital Simulation & Layout







- Full-custom environment
- Digital and custom co-design
- Fastest AMS simulation



- High-performance FastSPICE
- Multi-threaded golden HSPICE
- Multi-CPU accelerated SPICE



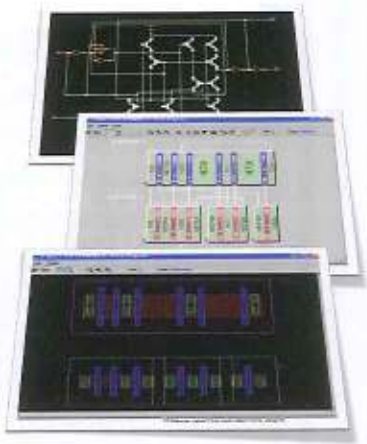
- IR, EM, aging analysis
- Device modeling leadership
- Advanced-Node Layout

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Synopsys Laker Custom IC Solution

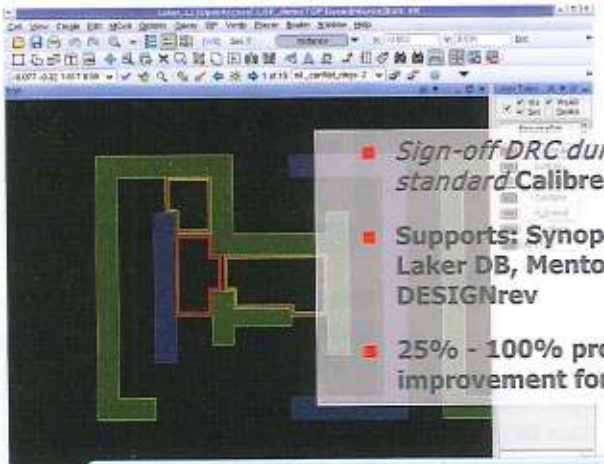
High performance, High capacity layout

- Advanced device generation
 - Full support for iPDK
 - Built-in Mcells
 - Template-based multi-device layout
- Rule-driven layout
 - Design rule checking, display and snapping during layout editing
- Schematic-driven layout
 - Connectivity guides fast construction of complex layout
 - Comprehensive mix of interactive and automatic routing
 - Works from all existing OA schematic tools



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Calibre RealTime and Synopsys Laker



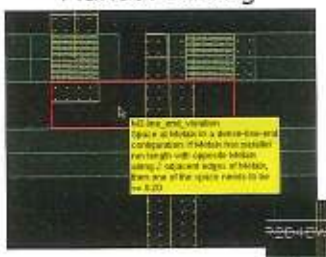
- *Sign-off DRC during edit*, **using *standard* Calibre decks**
- **Supports: Synopsys Laker OA, Laker DB, Mentor's Pyxis, Mentor DESIGNrev**
- **25% - 100% productivity improvement for 20 & 16nm layout**

Calibre RealTime – better layout in less time

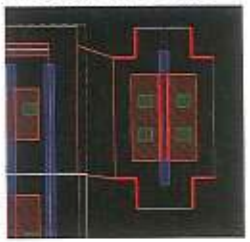
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RealTime – As You Edit

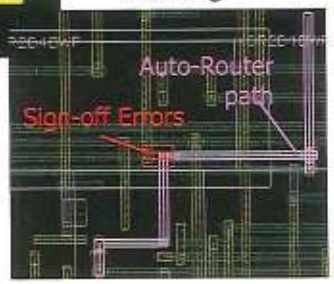
Manual Editing



MCells & PCells



Routing



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best electronic design 2011

Elektra2012 WINNER

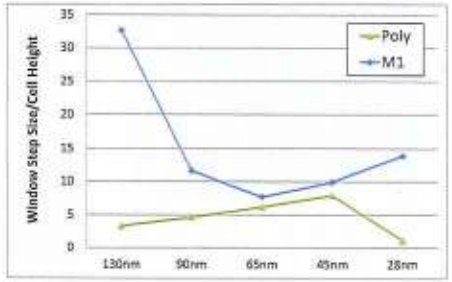
DESIGNVISION AWARDS - 2012 -

"THE TOOL WAS CLEARLY DESIGNED BY SOMEONE WITH FIRST-HAND ANALOG LAYOUT EXPERIENCE IN THAT IT NEVER SEEMS TO BE IN THE WAY, BUT YET IS ALWAYS AVAILABLE TO BE USED WHEN AND HOW THE DESIGNER WANTS TO USE IT."

Ted Buchwald, Sr. Engineer
Mobius Semiconductor

Signoff Verification During Design

- What's in a full sign-off deck?
 - Base geometry
 - Device rules
 - Lithography-driven rules
 - Density
 - Connectivity
 - ESD
 - DFM
 - Double patterning
 - Voltage-dependent DRC



- Even density rules are becoming a challenge

At 16nm, designers need full signoff feedback to optimize the layout

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Rules Unique to DP

- Odd Path Checks
 - Odd cycle with spacing < same mask rules are forbidden



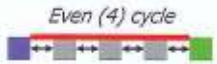
- Anchor Path Checks
 - Two polygons "anchored" to the same mask with an odd cycle path between them with spacing < same mask rules are forbidden

Odd (5) cycle



 - Two polygons "anchored" to opposite mask with an even cycle path between them with spacing < same mask rules are forbidden

Even (4) cycle

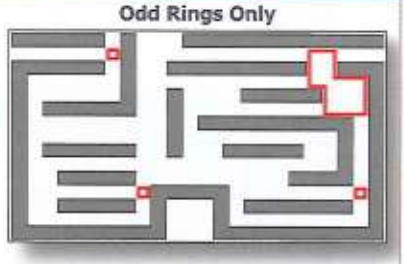


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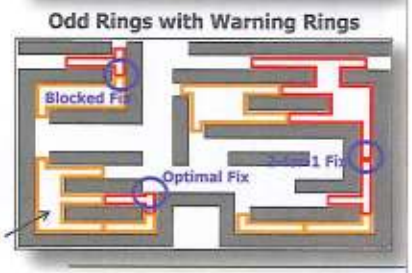
Calibre Multi-Patterning

Faster Debug with Patented Warning Rings

- DP & DRC errors are different
 - Long range
 - Mitigation with the right design methodology choices
 - Training is *essential*



- Odd rings only: wack-a-mole



- Warning rings: rapid debug
 - Enable with a minor deck change

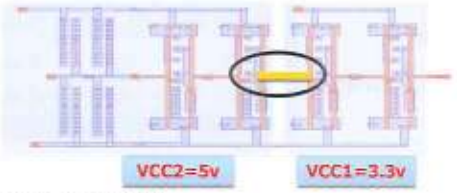
Warning Rings are Mentor Graphics Patent Pending

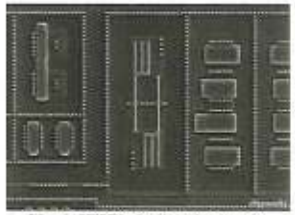
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VOLTAGE DEPENDENT DRC

Advanced nodes bring new requirements

- More voltage domains
- Desire to reduce spacing restrictions
 - — Spacing by voltage difference, not max voltage
- Marker layers become unmanageable
 - — Nets travel across domains
 - — Difficult to isolate by marker
- Text based methodology introduced

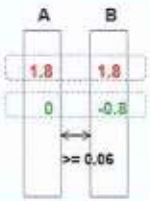




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More Accurate Approach: Voltage Annotations

- Migration to annotating text onto the desig to represent different voltages
- Enables lines with closer voltage swings to placed closer together



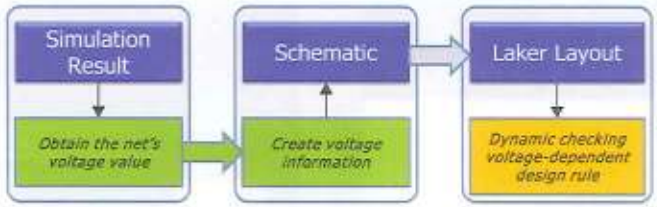
Nets	High	Low	Delta	Violation
A-B	1.8	-0.8	2.6	X
B-A	1.8	0	1.8	Y

- Only issue...
 - — How to reliably get the text representing voltages reliably on the design

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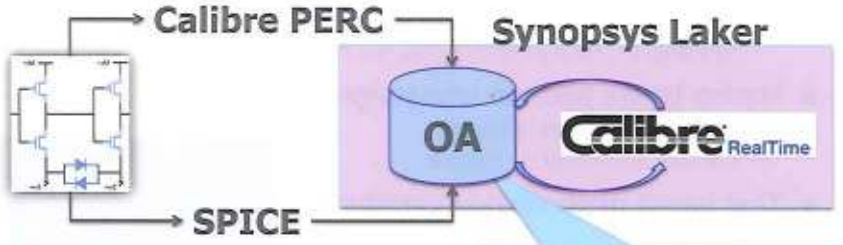
RealTime VD-DRC from Simulation
Latest joint work

- *Flow:* extract voltages from SPICE simulation and apply to the polygons *automatically* during edits
- Directly connects electrical and physical domains
- More than just verification – design enablement



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RealTime Roadmap: Voltage-dependent DRC



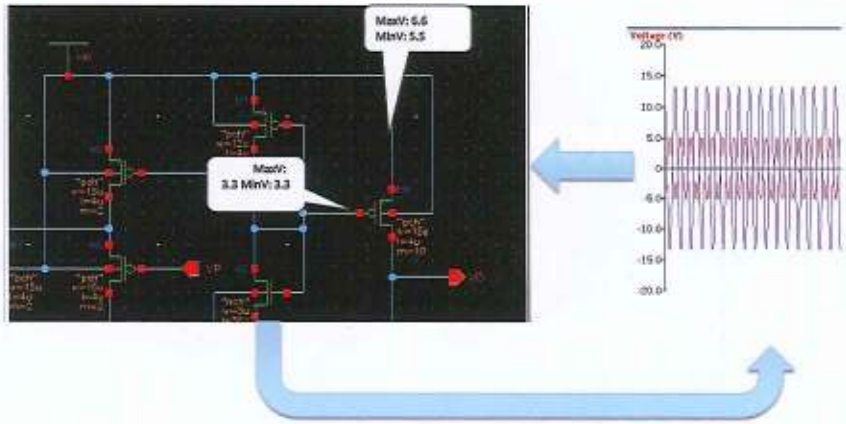
- Max/min voltages stored in OpenAccess constraints view
- Automatically generate text when running Calibre RealTime

Net name	Low V	High V
NetA	1.5V	1.8V
NetB	0.3V	3.3V
NetC	-0.5V	1.5V

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Calibre RealTime VD-DRC Checking

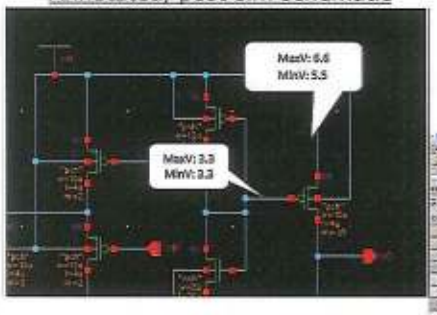
Schematic



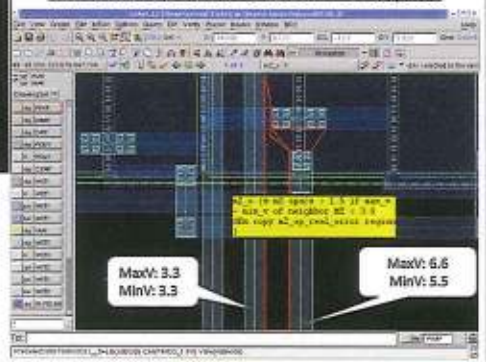
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Calibre RealTime VD-DRC Checking

Annotated, post-sim schematic



Annotated, schematic-driven layout



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NOTE

Implementing Secure SOC Devices

Analog Bits

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

Secure SOC devices are becoming are of increasing importance, across more markets and applications such as smartphones, tablets, network processors and IOT products. This paper will discuss a new approach to achieving higher-levels of tamper resistance, through the use of mixed-signal clock and sensor technologies.

As a consequence, improved hacker-resistance can be achieved with no impact to size or power and lowering the overall system costs. The technology behind a Secure Clocking and Sensor IP Core will be discussed, in addition to examples of usage in modern SOC applications.

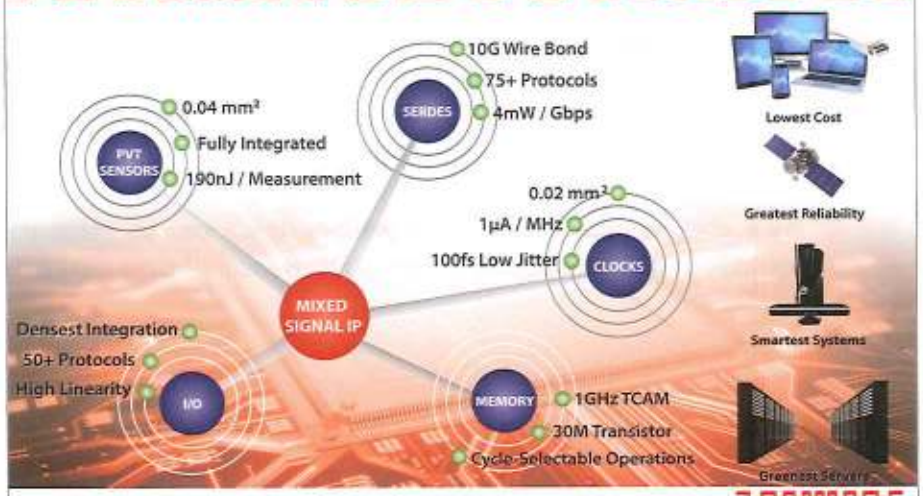
TSMC
Open Innovation Platform

Creating highly secure SOC implementations utilizing a secure-clock core

Alan Rogers - President & CTO, Analog Bits

Unparalleled Power Performance ANALOG BITS

Broadest Portfolio of Differentiated IP
Billions in Silicon



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Energy Efficiency and Security is Pervasive



- Every gadget and appliance should care about energy efficiency
- Every device needs to be secure

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Rising Demand for SOC Security

- Proliferation of network-connected devices
- Confidential information flowing through many devices

⇒A growing variety of consumer devices are gaining access to secure data

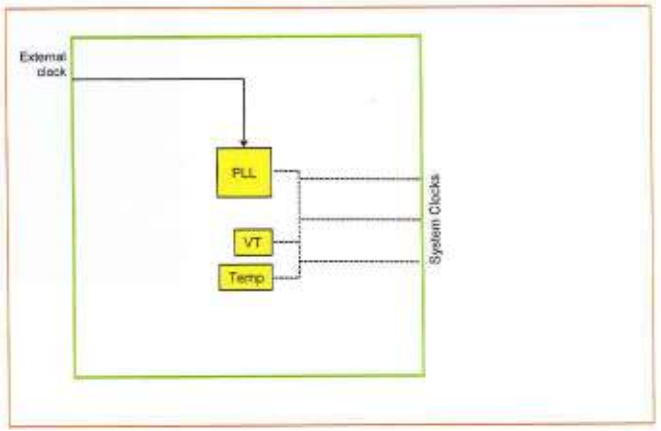
 - Smart phones
 - Tablets
 - NFC ("Secure element")
 - IOT devices
 - Your thermostats know if you are home or not!
 - And even your television is watching you!

Unparalleled Power Performance ANALOG BITS

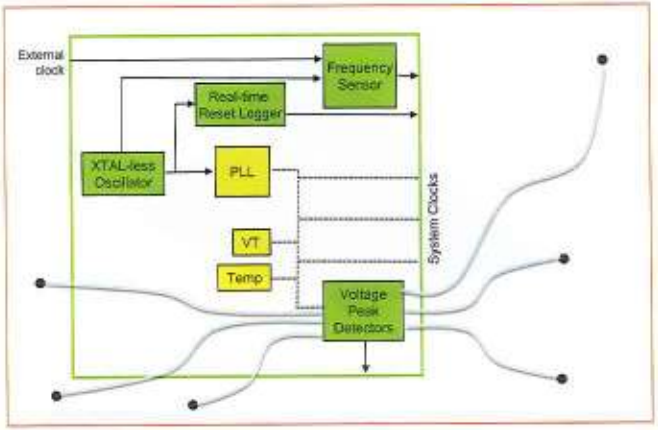
Hardware Hacking of SoC's

- By Voltage Manipulation
 - Under-voltage or over-voltage for functional and performance manipulation
 - Changing voltage on certain parts/domains of a SoC to cause a partial reset without losing data
- By Clock Manipulation
 - Real Time Clocks can be over-clocked or under-clocked
 - Once stopped, data can be read from memories, scan, etc.
 - This allows a SoC to be interrogated or even re-programmed at multiple points

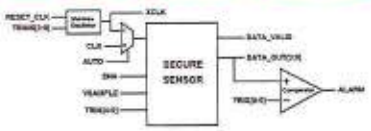
Current Status of Sensors

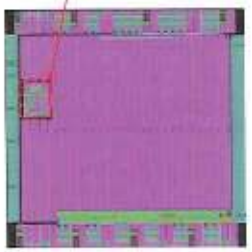


Achieving Tighter Security



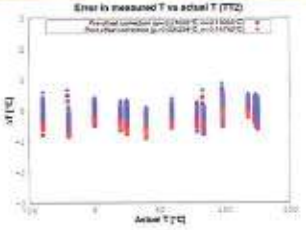
Collaboration with TSMC on 28nm





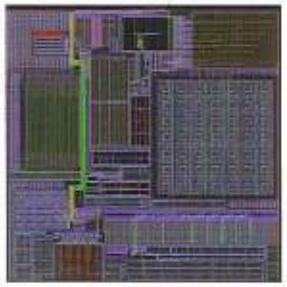
CLN28HPM Test Chip with Secure Sensor





Energy Efficient Security Tracking Sensor (1)

- Fully integrated on-die
- Monitors localized and remote
 - Process
 - Voltage: Power and Signal
 - Temperature
 - Clock integrity
 - Other proprietary secure functions



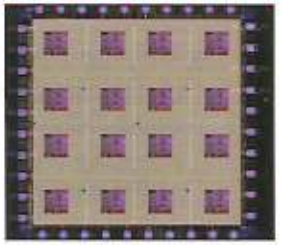
Fully Integrated Clock, Process, Voltage, Time and Temperature Monitors

Available in TSMC 40nm, 28nm, 20nm, and soon in 16FF processes

Unparalleled Power Performance ANALOG BITS

Energy Efficient Security Tracking Sensor (2)

- Lowest power – 190nJ/measurement
- Small core area – 200µm x 200µm

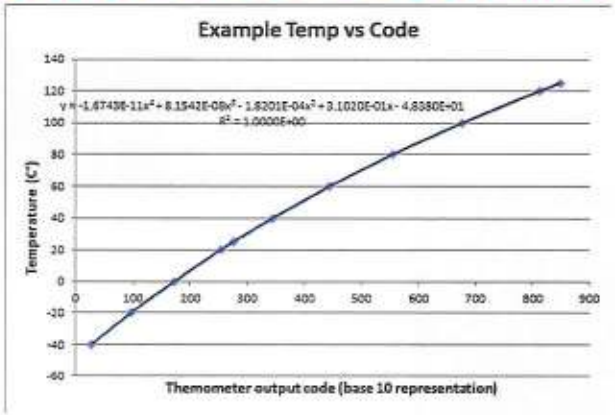


20SoC Sensors on a 2mm-square Test Chip

- ***Detects voltage spikes during security hacks***
- ***Reduces life-time failures by managing power density***
- ***Enables SW tracking of security violations***
- ***Continuously thwarts hardware attack in real time***

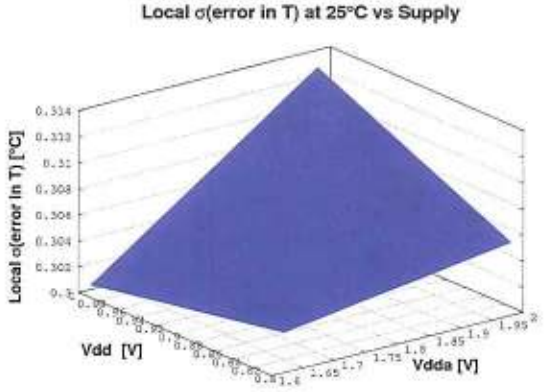
Unparalleled Power Performance ANALOG BITS

Secure Sensor Silicon Measurements (1)



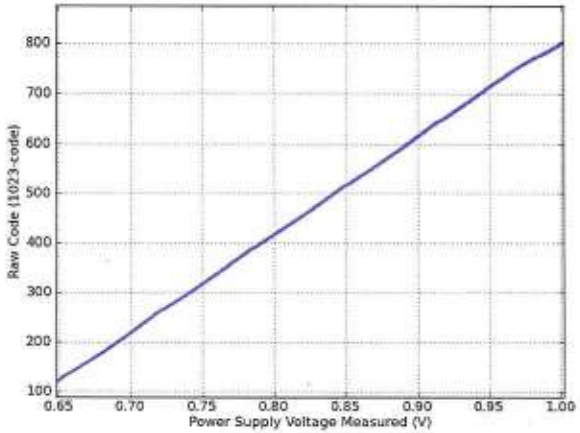
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Secure Sensor Silicon Measurements (2)



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Secure Sensor Silicon Measurements (3)



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Analog Bits and TSMC Collaboration

- Early access to advanced process rules - 20nm, 16FF
- Test chip collaboration in 28nm, 20nm and 16FF
- Extensive corner lot characterization with split lots
- Fully automated test characterization



Test Board includes an FPGA with PC USB interface for ATE

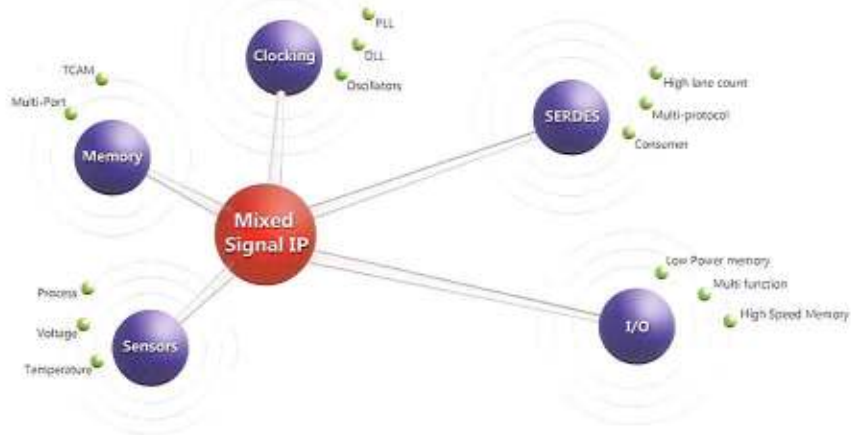
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Summary

- SOC-level security is an important consideration
- Secure Subsystems can be used to prevent:
 - Clock manipulation
 - Voltage manipulation
- Other aspects of SoC operation can be monitored in stealth
 - Tracking and preventing other forms of attack
 - Kept confidential from everyone but the customer
- Minimal impact to size and power

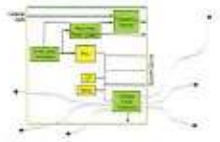
Unparalleled Power Performance ANALOG BITS

Industry Leader in Mixed-Signal IP
Billions in Silicon

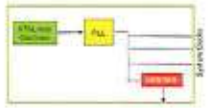


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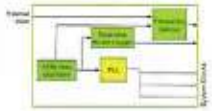
New Family of Secure Subsystems



Secure Sensor Subsystem



Secure SerDes Subsystem



Secure Clocking Subsystem

Unparalleled Power Performance ANALOG BITS

A Lasting Relationship
35+ Processes, 200+ Customers, 500+ Products

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Spanning three decades

Come see the TSMC 28nm/20nm Security IP demonstration at the Analog Bits booth

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NOTE

Electrostatic Discharge (ESD) Protection Guidelines for 40nm, 28nm and 20nm CMOS Designs

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ABSTRACT

FPGAs or ICs for computing, graphics or network applications typically use advanced CMOS technology for the optimal performance per power ratio and lowest cost per transistor. Clearly, TSMC's advanced CMOS platforms are well suited for these demanding applications.

While shrinking the transistor size can strongly reduce the cost it also reduces the maximum current and voltage tolerances. At 28nm the maximum voltage on the core transistors (even for short pulses in the 10ns range) is less than 4V.

Therefore, to saveguard their multi million dollar design investment designers need confidence that the end product survives all kinds of stress events during assembly and user handling. While there are several reliability considerations, this presentation summarizes electrostatic discharge (ESD) threats and solutions in advanced CMOS nodes like 40nm, 28nm and 20nm. Fortunately, many of the general purpose I/Os are adequately protected by TSMC's ESD protection cells included in the I/O libraries. However, for a range of specialty interfaces the general purpose I/O's are not ideal and alternative clamp concepts are required.

The presentation first provides an overview of the ESD related challenges in 40nm, 28nm and 20nm and future nodes. Different ESD protection concepts used in the industry are reviewed. Through a few case studies the audience will get guidelines to select the most appropriate concept for each interface type.

SOFICS
SOLUTIONS FOR ICs

ESD SOLUTIONS AT YOUR FINGERTIPS

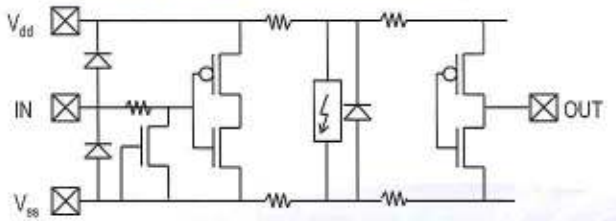
TSMC OIP – OCTOBER 2013

BENJAMIN VAN CAMP, DIRECTOR ENGINEERING

ELECTROSTATIC DISCHARGE (ESD) PROTECTION GUIDELINES FOR 40NM, 28NM AND 20NM CMOS DESIGNS

Traditional ESD solutions used in mature processes

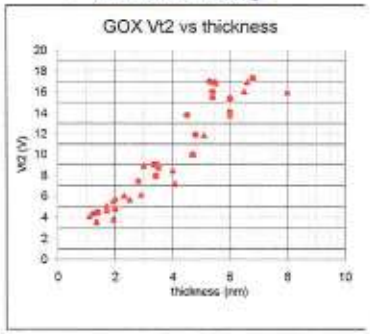
- Importance of ESD for IC industry
 - "Responsible for 20-30% of IC failures"
- Traditional ESD solutions
 - 'Dual diode' based protection
 - Self-protective output drivers (silicide blocked drains)
 - ggNMOS, LVTSCR clamps
 - Secondary protection – isolation resistance

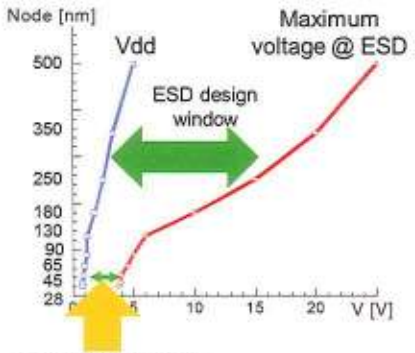


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Problem 1: advanced circuits easily fail during ESD

- Maximum voltage decreases
 - Transient breakdown of gate oxides
 - Burn-out of output drivers
 - Core failure voltage

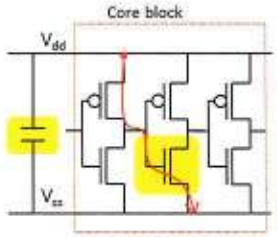




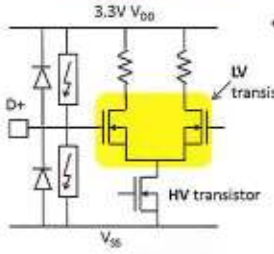
40nm/28nm/20nm:
ESD design space reduced to 3V!

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Sensitive thin oxide transistors under ESD stress



- On-chip decoupling capacitors
 - Stabilize Vdd supply potential
 - Reduce board level components: BOM
 - GOX1 capacitance: highest Cap/area
 - Reduced ESD design margin

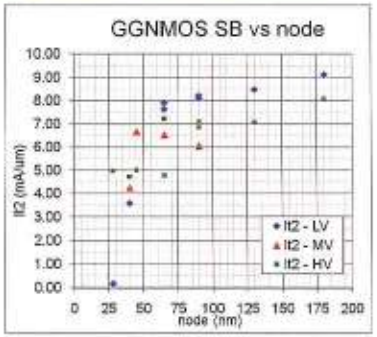


- Thin oxide transistors used in interface circuits
 - Analog tricks to improve circuit speed
 - Include core transistors in 3.3V domain
 - Designers use GOX1 transistor for speed reasons
 - Reduced ESD design margin

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Problem 2: Traditional solutions run out of steam

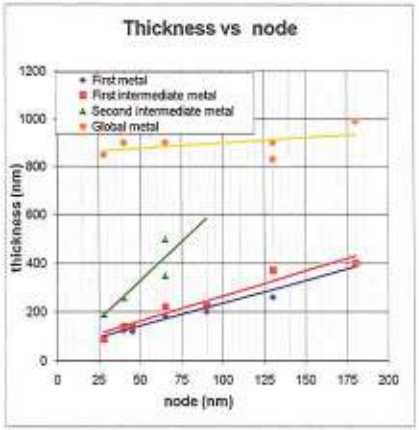
- (GG)NMOS:
 - Strong decrease in performance for 65nm and below
 - 28nm: SB GGNMOS **does not survive snapback**
- Diodes
 - 35mA per micron up to 65nm
 - Severe drop in performance in 40nm, 28nm
 - Capacitive loading increases



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Problem 3: Metallization constraints in adv. CMOS

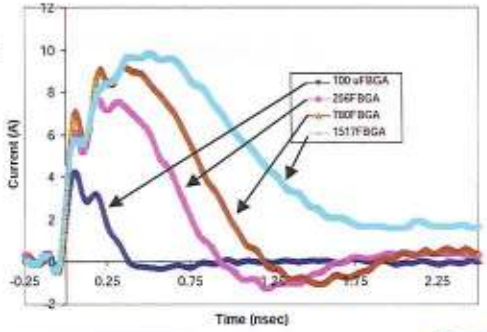
- 2 groups of metallization
 - Local metals get thinner (400%)
 - Top metal thickness remains
- Influence on ESD robustness
 - ESD robust power bus still possible
 - Top metal layers remain thick
 - But additional constraints:
 - Connections to power bus
 - Internal connections inside the ESD clamp



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Problem 4: CDM current increases for Large SoC's

- 500V CDM stress – transient current waveform
 - Strong dependence on package type, size
 - Rise time increase
 - Pulse width increase
 - Current amplitude increase
 - Large pin count SoC's
 - Need more robust ESD



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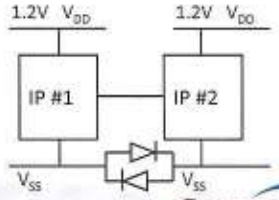
Problem 5: Combining different vendor's IP

- SoC combines IP from different IP vendors
 - IP block 1: Within specs
 - Fully qualified for ESD protection
 - Silicon proven, product proven
 - IP block 2: Above specs
 - Fully qualified for ESD protection
 - Silicon proven, product proven
 - Wired together in SoC: Below spec
 - Functionality: OK
 - ESD qualification: below spec!
 - Who is responsible?

Full product
<1kV HBM,
<100V CDM

IP#1 alone
>2kV HBM,
>500V CDM

IP#2 alone
>4kV HBM,
>1000V CDM



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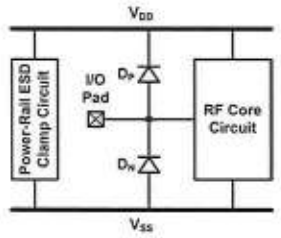
Problem 6: Higher ESD thresholds for selected pins

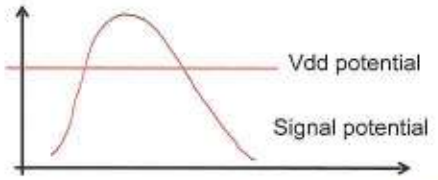
- Different interface types
 - Internal connections
 - Within package, between different substrates or to integrated antenna
 - Reduced ESD threshold can suffice: <1kV HBM
 - IC-to-IC connections
 - On the same PCB, module
 - Standard ESD protection for safe assembly: 1kV to 2kV HBM
 - External connections
 - To other sub-systems
 - USB, HDMI, ...
 - Higher ESD threshold required: sometimes even 8kV IEC 61000-4-2 required

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Problem 7: Higher voltage tolerance for selected pins

- Traditional ESD solutions limits I/O voltage swings
 - Higher voltages required for chip-to-chip communications
 - Hot swap, fail safe, over voltage tolerant requirements
 - Back drive protection





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TSMC – Sofics cooperation

- History
 - 2008: Design Center Alliance Partner
 - 2010: TSMC Licenses Sofics PowerQubic™ Technology for 0.25-micron BCD Process
 - 2010: IP Alliance Partner
 - 2011: First libraries approved (LQMP) and online
 - **2013: Several libraries available at TSMC online: 65nm, 40nm, 28nm**
- **Sofics serves 30+ TSMC customers**
 - Sofics solutions complement foundry clamps
 - TakeCharge: any CMOS down to 28nm
 - 0.18-micron 0.13-micron 90nm
 - 65nm 40nm 28nm
 - PowerQubic: from 0.35 to 0.18-micron BCD
 - 0.35-micron High voltage
 - 0.25-micron BCD Gen I and II
 - 0.18-micron BCD Gen I and II

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Specialty ESD clamps available on TSMC technology

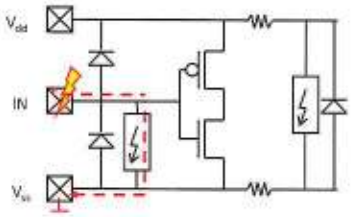
- Broad solution coverage on TSMC technology
 - Silicon proven solutions, including different flavours
 - > 250 silicon proven cells – datasheets available online
 - **Portable to other nodes/domains**

Node	Voltage domains
350nm HV	3.3V, 15V
250nm BCD, gen. I and II	12V, 24V, 40V, 60V
180nm BCD, gen. I and II	18V, 24V, 32V, 40V, 60V
180nm CMOS	1.8V, 3.3V, 5V
130nm CMOS	1.0V, 1.2V, 3.3V, 5V, 7V
90nm CMOS	1.2V, 1.8V, 3.3V
65nm CMOS	1.0V, 1.2V, 1.8V, 2.5V, 3.3V, 5V
40nm CMOS	0.9V, 1.2V, 1.8V, 3.3V, 5V
28nm CMOS	0.85V, 0.9V, 1.8V, 3.3V, 5V, 5.5V, 12V

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Solution: Local I/O clamp reduces total voltage drop

- Local I/O clamps
 - Strongly reduce voltage drop during ESD
 - Protect extremely sensitive nodes
 - Reduced dependence on bus resistance
 - Many different device options
 - Optimize for each interface type
 - Allow higher voltage
 - Allow higher ESD threshold
 - Allow reduced capacitance
 - For wireless or high speed interfaces

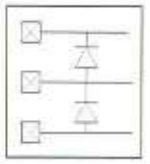


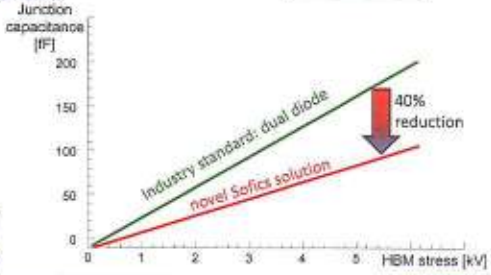
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Example: Low capacitance ESD solutions

- Lower parasitic capacitance can enable higher datarate
 - Traditional I/O-ESD protection
 - Dual diode
 - GPIO and high-speed/RF I/Os
 - Various clamps with low cap available
 - Example: TSMC 28nm **28Gbps** protected by Sofics DTSCR
 Cap = 80fF including metal and reverse diode
 - Sofics newest innovation:
 - Reduce capacitance by 40%
 - Silicon proven in 65nm, 28nm
 - Reduced cap for same ESD
 - Verified on VF-TLP for CDM



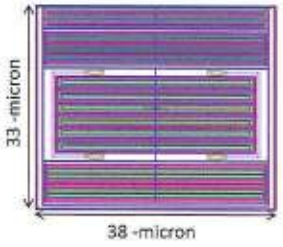


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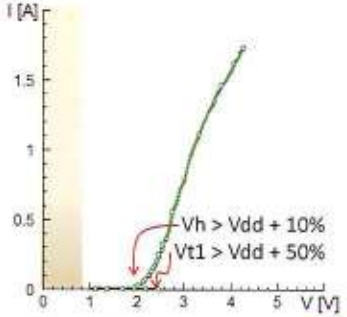
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Example: 40nm thin oxide transistors protection

- Solving several challenges
 - 40nm CMOS – 0.9V domain
 - 3.6kV HBM
 - 245V MM
 - < 100pA leakage



40nm 0.9V power clamp example

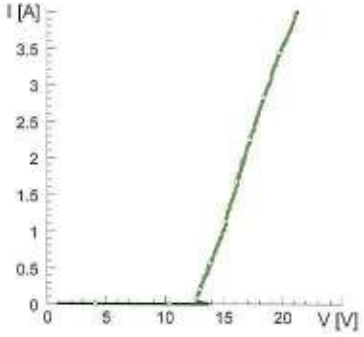


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Example: 28nm 13V PowerQubic device

- Tolerates high voltage in advanced CMOS
 - Size: 59um x 80um
 - Leakage
 - 30 nA (Room temperature)
 - 100 nA (125°C)
 - Holding voltage
 - 14 V (Room temperature)
 - 14 V (125°C)



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Example: Meet severe reliability requirements

- Sofics solutions meet severe requirements
 - Component level **ESD** or system level ESD
 - 8kV HBM, 800V MM – HDMI, Timing controllers
 - 8kV IEC 61000-4-2 – USB 2.0, analog switches, HDMI
 - **EOS** compatibility examples
 - 14V IEC 61000-4-5
 - 45V ISO 7637-2 pulse 5
 - **Latch-up** and transient latch-up
 - ESD under powered conditions

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Conclusion: On-chip ESD clamps available

- Key challenge for IC applications: on-chip ESD protection
 - Risk of destruction of semiconductor devices
- Provided an overview of the challenges in advanced CMOS
 - Sensitive transistors, metallization constraints, SoC complexity
- Provided solutions
 - Local protection based on proprietary clamps
- Introduced Sofics ESD solutions
 - Flexible IP portfolio to address various requirements
 - Technical and financial benefits
 - Verified and available on many TSMC platforms

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NOTE

Circuit Reliability Simulation with TSMC TMI Age Model

Cadence

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

As device size continues scaling down, reliability effects such as Hot-Carrier Injection (HCI) and Bias Temperature Instability (BTI) become major concerns. These effects cause device degradation which will lead to circuit performance degradation, yield loss or even circuit failures. It is imperative to consider these effects in design and sign-off validation.

TMI is TSMC Model Interface that is a C language based modeling API developed to support extensions of standard compact models, like BSIM4, BSIMCMG, etc. TMI was selected as standard SPICE model API by CMC (Compact Model Council). TMI has several functionalities, like customization of LDE (layout dependent effect), additional SPICE modeling effects on top of standard SPICE model, etc. TMI also supports TSMC reliability aging model.

TSMC has begun to ship TMI aging models for 28nm process or below. Cadence worked with TSMC to integrate TMI aging model into Cadence Virtuoso simulators. In this session, we explain what is reliability simulation, TMI aging flow, and how to run TMI aging models with Virtuoso® RelXpert, Spectre/APS/XPS native reliability simulation, and how to setup and run reliability simulation with Analog Design Environment (ADE).

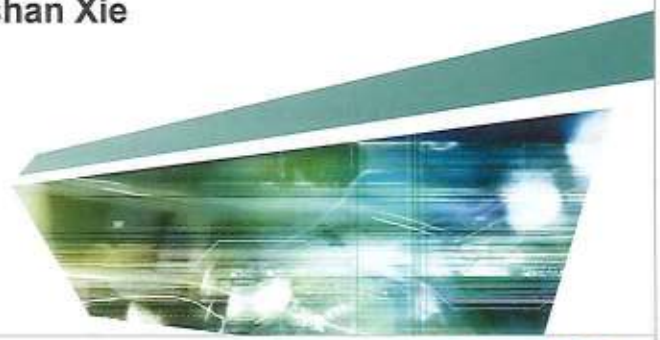
TMI aging flow supports both conventional SPICE transistor level and fast-SPICE simulation. In the conventional SPICE simulation flow, two stage analyses are performed. The first stage is stressing the devices to calculate device degradation, and the second stage uses the degraded device model to perform aging simulation that can predict circuit behavior and performance after certain years. Fast-SPICE targets large circuit with millions of transistors. Since each transistor may have different stressing condition, each device may generate a degraded SPICE model card. This poses serious issue in memory and capacity for very large circuit for fast-SPICE. Working with TSMC, new TMI APIs are proposed to address fast-SPICE reliability simulation issues. This paper describes both SPICE and fast-SPICE TMI aging simulation flows, it also introduces TMI reliability simulation into ADE environment through RelXpert and Spectre/APS/XPS. It allows user to set various options for TMI-aging flow simulation and output various results such as fresh and degraded waveform comparison, highlight hot spots and back-annotate results to schematic. Example cases and simulation results are presented.

As reliability becomes more important and a necessary for designs, TMI-aging flow allows customer to perform reliability simulation to ensure design in reliability.

INVENTIVE

Circuit Reliability Simulation with TSMC TMI Age Model

Jushan Xie



2013 Open Innovation Platform ECOSYSTEM FORUM

Outline

- Why reliability is important for circuit design
 - HCI and NBTI/PBTI
- TMI feature
- TMI reliability
 - TMI reliability
 - TMI ADE integration
 - TMI Fast-SPICE integration
- Summary

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Nobody wants to buy an unreliable product!

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Integrated Circuit Failure Modes

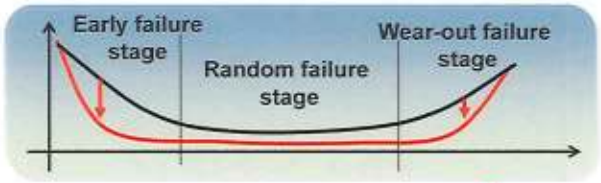
Failure Mechanisms

- Early failure stage
 - Open / Short
 - High Resistivity
 - Leakage
- Random Failure Stage
 - Cross Talk
 - Delay / Act Failure
 - I_{DDQ}
- Wear-Out Failure Stage
 - HCI, NBTI, PBTI, TDDB
 - Interconnect Electro migration

Marginal device failures
Manufacturing/process failures

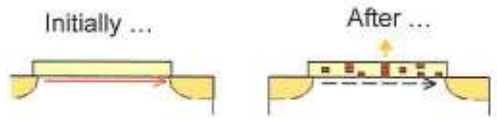
Design "corner" failures
Statistical analysis failures

Wear out, device aging failures
Device degradation failures



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MOSFETWearout Failure Mechanisms



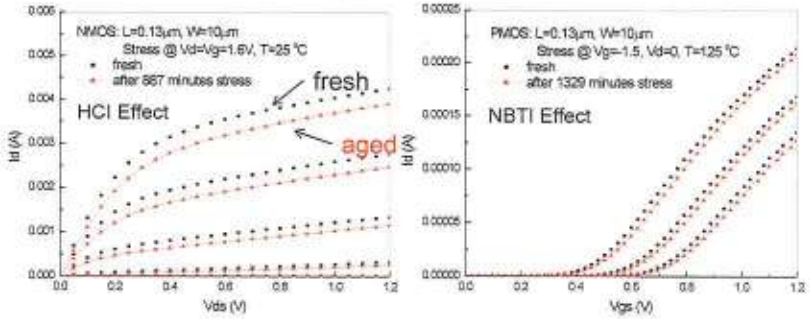
Si-H bonds failure:	Hot Carrier Injection Degradation (HCI) Negative Bias Temperature Instability (NBTI/PMOS) Positive Bias Temperature Instability (PBTI/NMOS)
Si-O bonds failure:	Time Dependent Dielectric Breakdown (TDDB)

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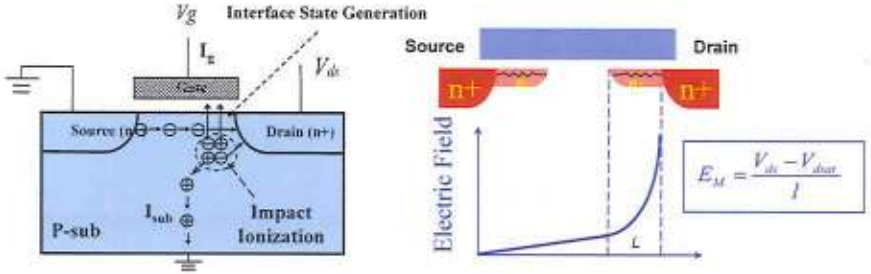
Impact Device Characteristics

- MOSFET characteristics degrades
 - Lower current → slower circuits!
 - Gm degradation and Vth shift → big issues for analog applications
- HCI, NBTI, PBTI are major MOSFET device degradation mechanisms for advance process



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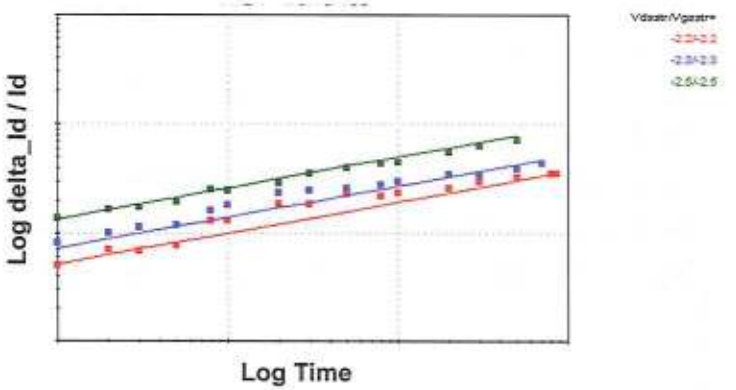
Hot Carrier Injection (HCI)



- Hot electrons accelerated by lateral electric field
- High energy electrons cause ionization
- Hot electrons are injected into gate-oxide and cause charge trap and generate interface states

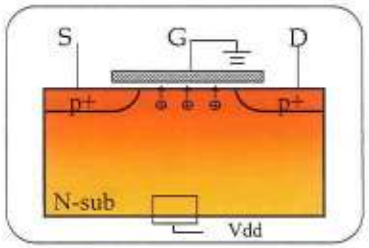
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Example HCI Stress Data



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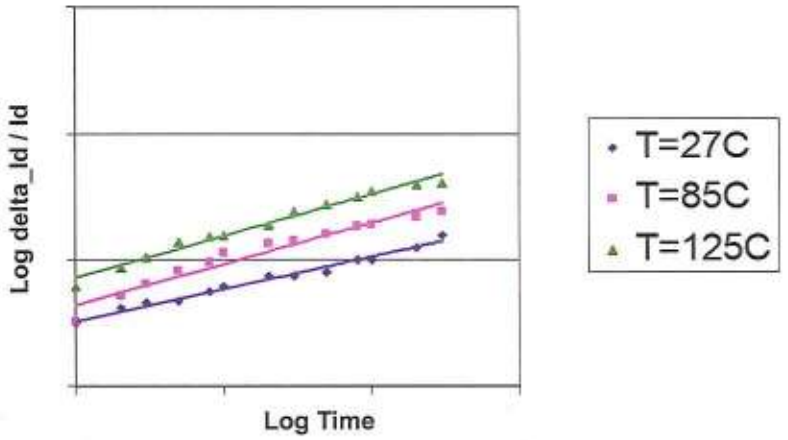
Negative Bias Temperature Instability (NBTI)/PBTI



- NBTI/PBTI:
 - Driven by high vertical electric field and accelerated by high temperature.
 - Cause interface-state generation at the Si/SiO2 interface.
- Challenges of NBTI/PBTI simulation
 - Need to model immediate failures unlike the long-term aging effect of HCI
 - Transistor characteristics can recover after failure

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Example NBTI Stress Data



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TMI (TSMC Model Interface)

- **TMI - TSMC Model Interface**
- **C based modeling API**
- **Built on top of standard compact SPICE modeling**
- **Customize standard compact models**
- **Backward compatible with standard models**
- **Support different simulators and platforms**

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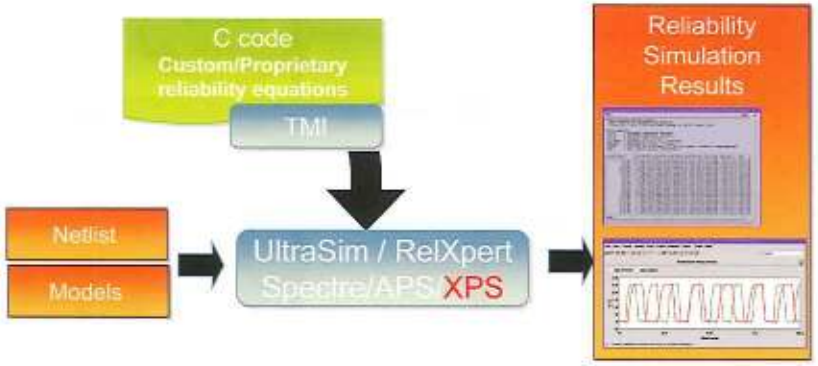
TMI Features

- **Flexible customized scaling for geometry and temperature.**
 - ➢ Additional instance and model parameters
 - ➢ Customized layout proximity effect, temperature effect, and statistical models
 - ➢ Flexibility and higher efficiency via TMI
- **Support flexible device topology**
 - ➢ Allows additional component(s) and internal node(s) on top of standard compact SPICE model
 - ➢ Customize model formulation
- **Support reliability aging modeling.**
 - ➢ Add customized aging model (algorithms, age integration, extrapolation)
- **Support SOA (Safe Operating Areas) check**

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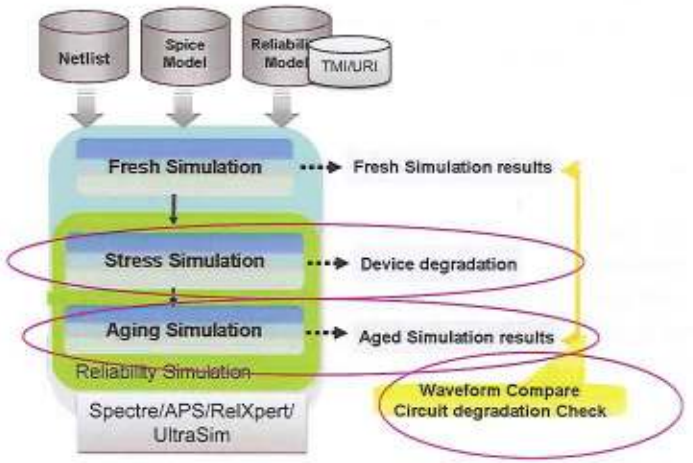
TMI-aging Modeling



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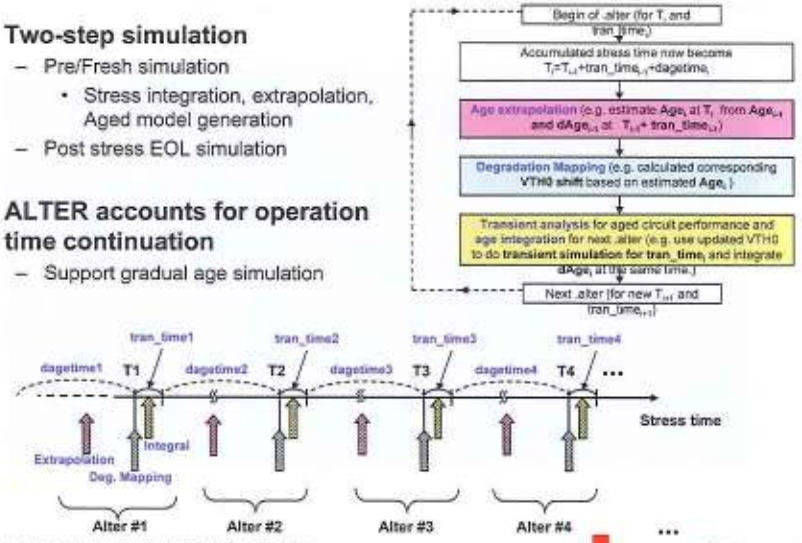
Reliability Simulation Flow



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TMI-aging Flow

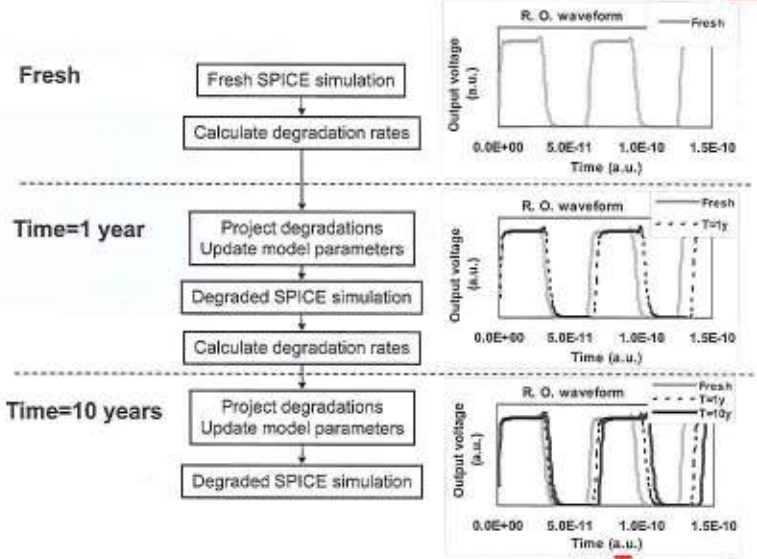
- **Two-step simulation**
 - Pre/Fresh simulation
 - Stress integration, extrapolation, Aged model generation
 - Post stress EOL simulation
- **ALTER accounts for operation time continuation**
 - Support gradual age simulation



(Initial Alter: the devices could be fresh or degraded from previous simulation.)

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TMI-aging Results



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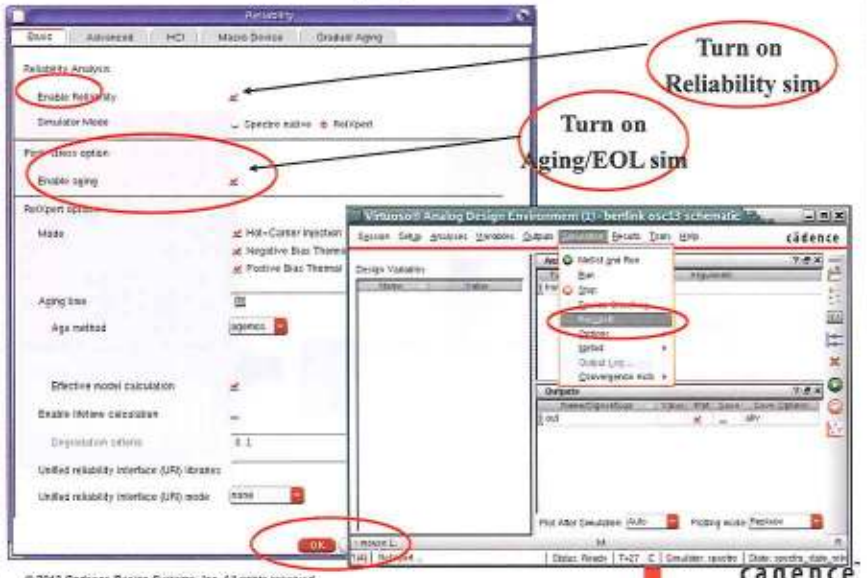
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TMI Support

- TSMC shippingTMI aging models for 28nm process amd below
- Cadence worked with TSMC to integrate TMI aging model into Cadence Virtuoso simulators
 - Spectre/APS
 - RelXpert
 - UltraSim
 - XPS
 - Analog Design Environment (ADE)
- User can control TMI-aging via RelXpert control statements or GUI interface
- With URI (User defined Interface), reliability simulation can extend to other MOSFET models (PSP, HISIM) or degradation mechanisms (TDDB)

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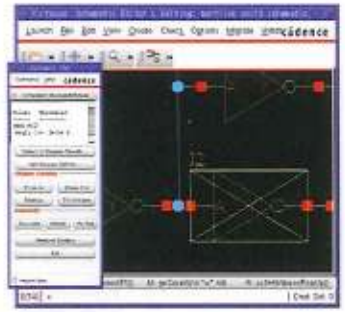
ADE Interface to run TMI-aging



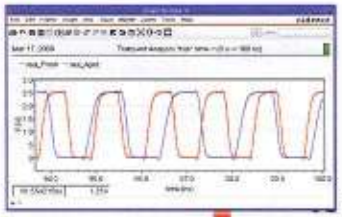
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ADE Interface
TMI-aging Reliability Analysis Results

- Schematic Cross Probing
 - Explorer in Schematic
- Waveform
 - Compare with Fresh and Degradation
- Text Report
 - Check Degradation Values

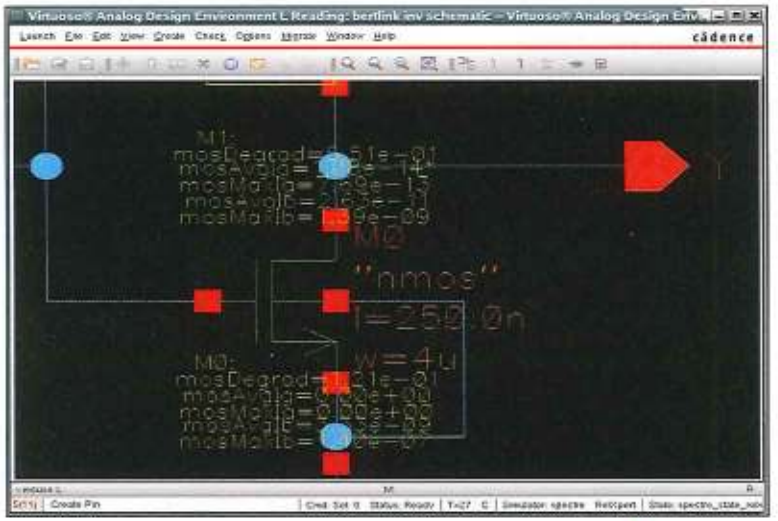






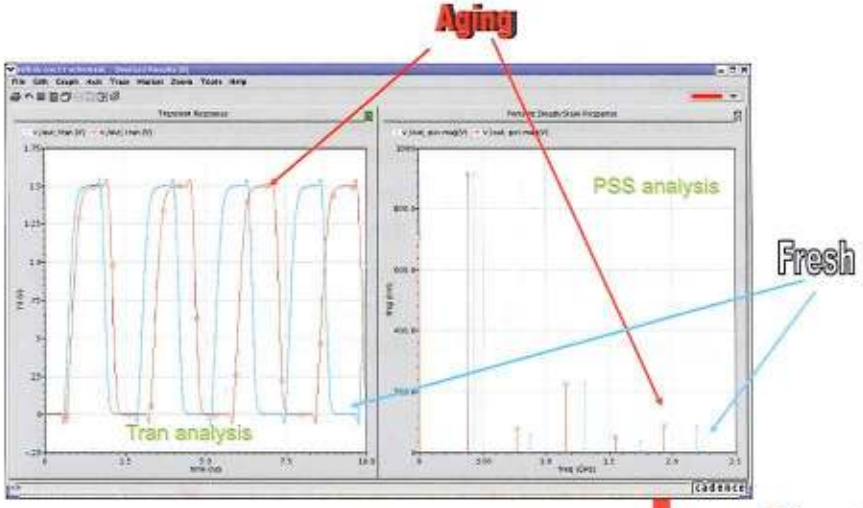
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Schematic Back-Annotate Degradation Results



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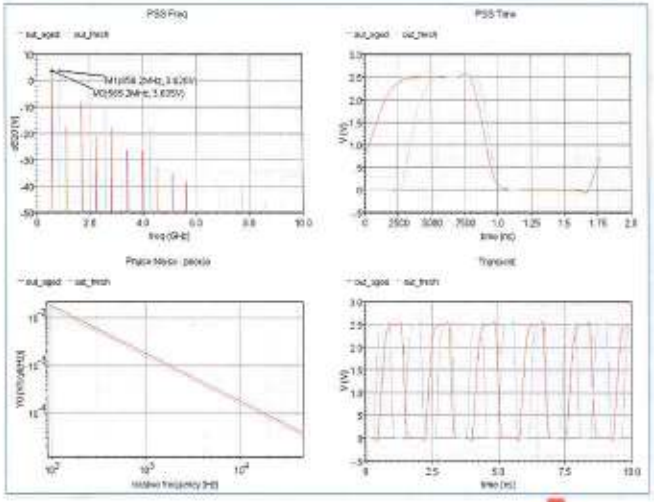
Running with Other Analysis
Spectre Tran & SpectreRF PSS Results



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Device Aging Simulation Example
Test Circuit Ring Oscillator

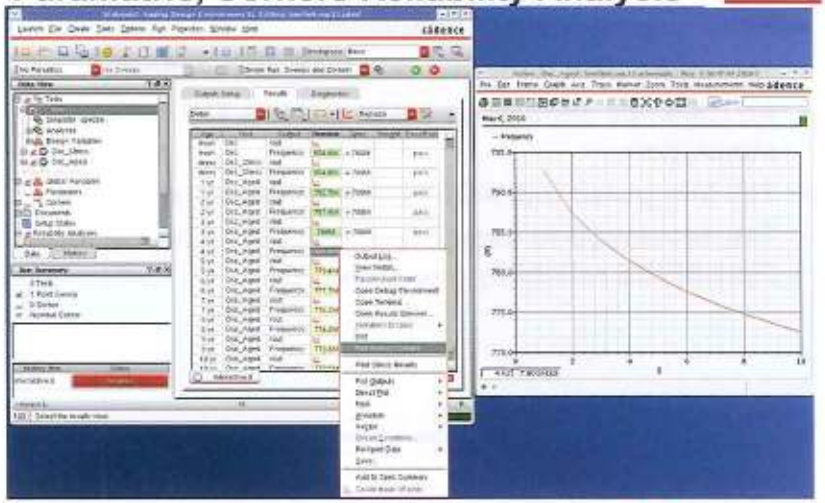


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ADE-XL: Allows Multiple Test Bench, Paramatric, Corners Reliability Analysis

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TMI for Fast-SPICE

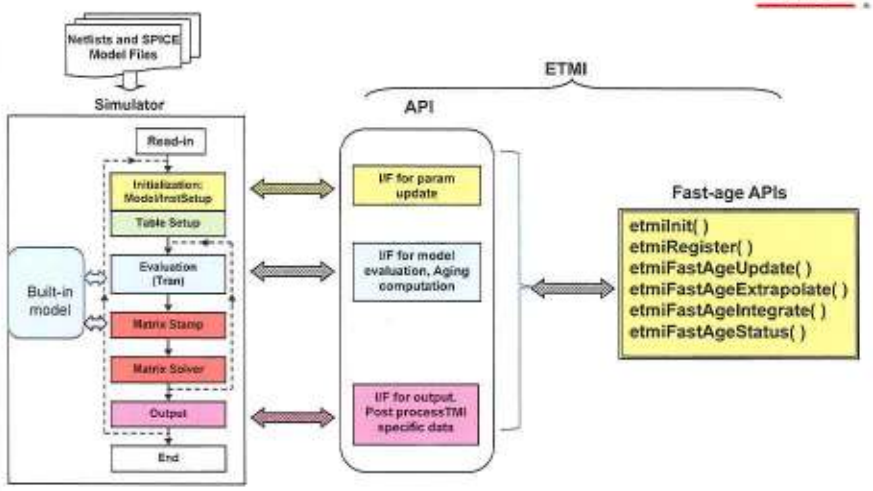
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- Conventional SPICE aging flow generates a new model for each degraded device
- Impractical for Fast-SPICE simulation with millions of transistors
- Cadence worked with TSMC to develop TMI API for Fast-SPICE aging

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ETMI Architecture for Fast-SPICE



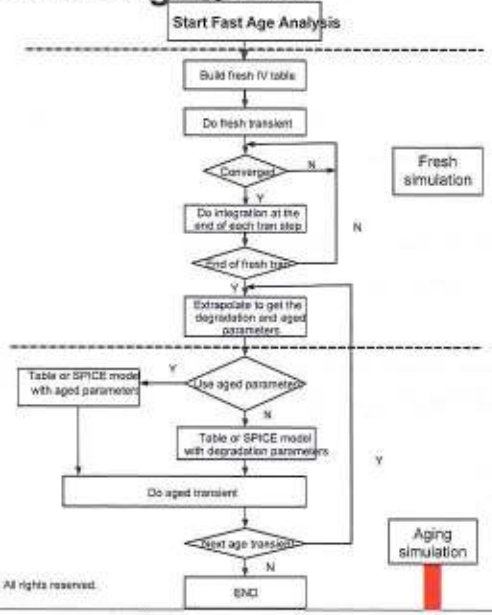
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Consideration for ETMI – Fast-SPICE Aging

- Fast simulators might use IV/CV tables for model evaluation
 - Not able to inform TMI side model/instance parameters during age integration and age extrapolation.
- Fast simulators might need degradation data from aging simulation to estimate aged device behavior
- Fast simulators also need additional information to know if aged devices could share IV curves so that simulator side can optimize the calculation and memory

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ETMI – Fast-SPICE Aging Flow



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Summary

- **Reliability analysis is important!**
- **TMI-aging flow performs reliability simulation**
- **All Cadence simulation tools perform TMI reliability simulation**
- **TMI integrated into ADE with full functionality**
- **TMI developed to overcome bottlenecks for perform Fast-SPICE reliability simulation**

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Acknowledgement

- **Cadence**
 Alvin Chen
 Yunpeng Pei
- **TSMC**
 Ke-wei Su
 YC Liang

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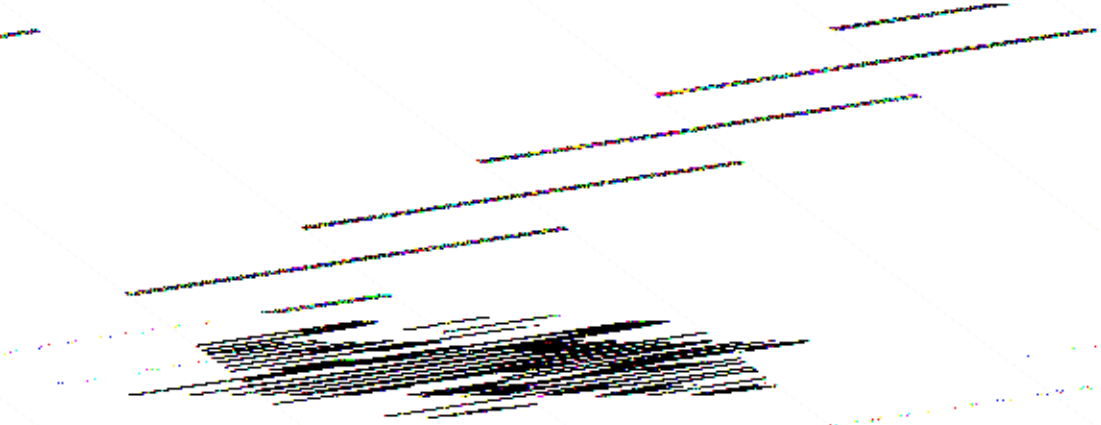
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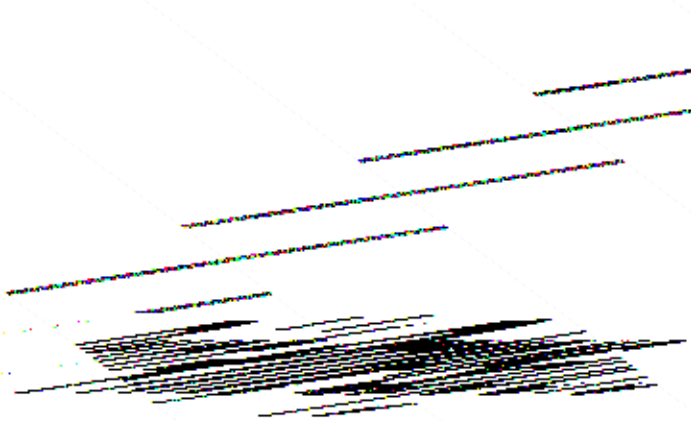
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NOTE





Verify TSMC 20nm Reliability Using Calibre PERC

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ABSTRACT

Semiconductor technology is aggressively advancing following Moore's Law, various reliability issues are risen due to shrink of geometry and increase of electrical stress. The impacts are on both FEOL and BEOL. For major reliability issues associated to (or through) BEOL, they are EM, SIV, TDDB of inter-metal dielectric, and CDM ESD in most advanced technology nodes. On EDA side, there are already well established EDA tools to handle EM and SIV issues. Here, Mentor presents Calibre PERC, as one tool platform to tackle verification of rules defined in TSMC N20 DRM for TDDB of inter-metal dielectric and CDM ESD reliability issues.

Calibre PERC performs Delta Voltage DRC which the rules are becoming very critical per TSMC N20 DRM Layout DRC guidelines. While TSMC has provided DRC rules to verify spacing of polygon shapes in maximum delta voltage, it is generally considered as designer's responsibility to assign the voltage label marker into layout database. When full chip simulation is not feasible to generate meaningful voltage labels, Calibre PERC provides "Voltage Aware DRC", which is one application of PERC-LDL DRC function, combines schematic "Voltage Propagation" function with LDL DRC to automatically generate voltage label annotation into desired geometry shapes on full chip. The result is a SVRF "Layout Text" file to be directly plugged in with TSMC provided delta voltage DRC rules. Even with TSMC revision of delta voltage DRC rules. The existed "Layout Text" file is good to plug into new revised deck.

CDM ESD damage on GOX is more observed in multi-power domains design if there is no intentional protection scheme or effective ESD route presented for 65nm and below technology nodes. It is becoming very critical in N20. TSMC has defined rule SPEC in DRM, but marked as "un-checkable". Calibre PERC, the only EDA tool with the solution to fully cover TSMC requirements, has been in close collaboration with TSMC IO/ESD team to develop automatic verification kit to verify CDM ESD issue for N20 node. Details for both verification methodologies will be presented.



Verify TSMC 20nm Reliability Using Calibre PERC

Frank Feng
Circuit Verification Methodologist
Yi-Ting Lee
Foundry Technical Marketing Engineer

D2S Calibre Marketing

Mentor Graphics

20nm Technology Node Reliability Issues
Various Causes

- Electrostatic Discharge (IO ESD and **CDM ESD**)
- Latch-Up (LUP)
- Electrical Overstress (EOS)
- Time Dependent Dielectric Breakdown (**TDDB**)
- Electromigration (EM)
- Negative Bias Temperature Instability (NBTI)
- Hot Carrier Injection (HCI)
- ...

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The Role Of Calibre PERC For Reliability Verification Design Automation

- Calibre PERC is mostly a static schematic and layout checker for user defined design rule guidelines to prevent reliability issue
- Calibre PERC work on
 - Layout and source netlist (spice and cdl)
 - Stream out database (GDSII & OASIS)
 - Design database (LEF/DEF)
- Calibre PERC is not a dynamic simulation tool
- Calibre PERC provides a rule based automation design solution for ESD/reliability check
 - Transform engineering ESD/reliability knowledge into rules
 - Replace manually repeated effort with an automatic checker

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Benefit For Reliability Verification Design Automation



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A Honest Comparison Using Calibre PERC Vs. Semi-Auto And Manual Only Check

- A design and sign-off solutions that remove doubt
 - — Clear defined rule spec and right tool to eliminate errors
 - — The "human" element is often the weakest link

Items	Calibre PERC	Marker Layers	Eye Ball
Rules Coverage	100%	under 30%	under 10%
False Error	no	many	always
Tool Integration	Topology, LVS, DRC, R-extraction	DRC + manual marker	manual examination
Tool Quality	sign-off level	dependence	no quality
Programmable	fully	partially	never
Run Time	minutes	minutes ~ hours	hours ~ days
Human Error	never	sometimes	always
User Usage	automatic	semi-auto	manual

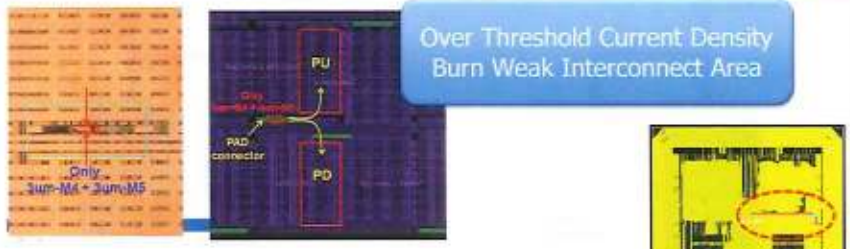
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Calibre PERC Is A Design Automation Tool For ESD and Reliability Verification → The Facts

- EOS cause multi-millions dollars loss is a critical issue in multi-power domain SoC chip design, big chip company implement PERC for static EOS check
- Mobile chip design house catch weak interconnect which fail the chip due to over threshold Current Density
- Design house catch device violating ERC which eventually will fail during burn-in
- TSMC announces relationship with Mentor on "ESD" solution at the 2013 Tech Symposium; production kit release planned for October

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Calibre PERC Measured Violation Matches Real Silicon Failure



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Calibre PERC Integrates Schematic Check That Cross Referenced To Layout Check

- Schematic Check
 - — Programmable **Topological Checking** syntax and subckt **Pattern Recognition** target on both standardized modularization and customization checks
 - — **Voltage Propagation** is particularly useful for **Gate Dangling** and **EOS** checks
- Logical Driven Layout (**LDL**) Check
 - — **P2P** effective Resistance checking
 - — **Current Density** checking
 - — **Net/Device based DRC** checking
 - — **Source based LDL** is doing layout check, and the layout check is correlated to circuit components originated from **source netlist**
 - — **Layout based LDL** is doing layout check, and the layout check is correlated to circuit components originated from **layout netlist**
- Advanced **PERC-RVE** Debug
 - — Easy-to-use and advanced debug gui interface for Calibre PERC

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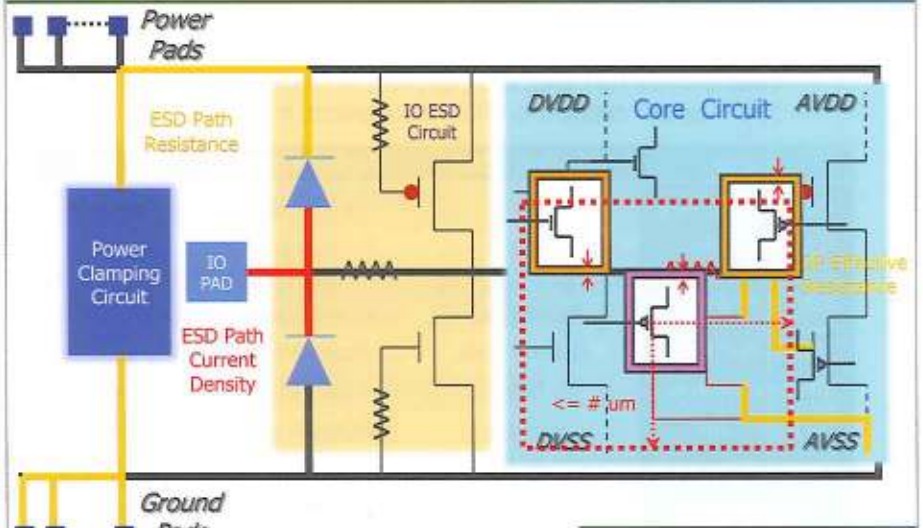
Calibre PERC Is A Platform

Provides Comprehensive Features To Handle Wide Scope Of Reliability Issues



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Calibre PERC Provides 360-Coverage For ESD/Latch-Up/Reliability Design Verification

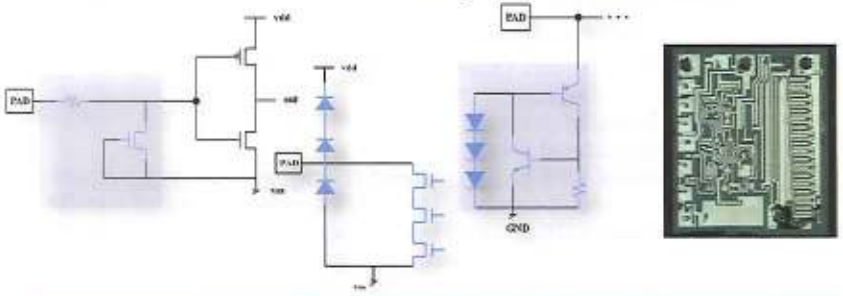


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Customization of IO ESD Protection Schemes

All can be Checked by Using Calibre PERC

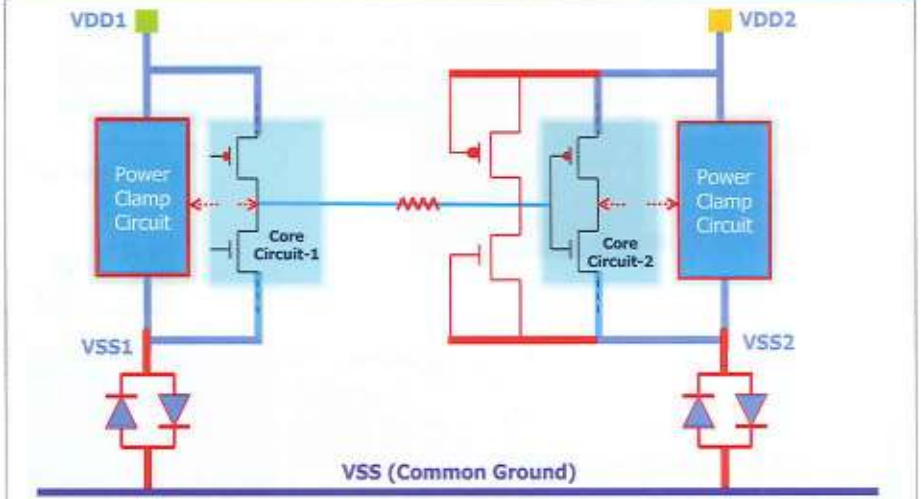
- Electrostatic discharge (ESD) causes severe damage to ICs
- Several protection schemes have been proposed to mitigate this damage
- User can use net/device connectivity tracing cmd in PERC, or using pattern match in PERC to check user defined good "protection schemes"



Checking for proper ESD protection circuits is needed for reliable design

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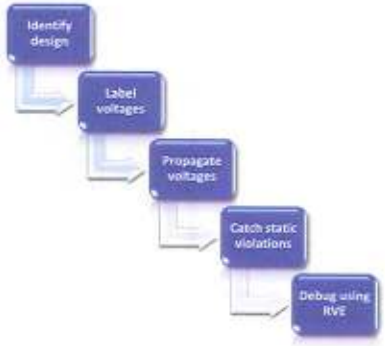
PERC Covers Complex CDM ESD Protection Schemes for Multi-Power Domains Design

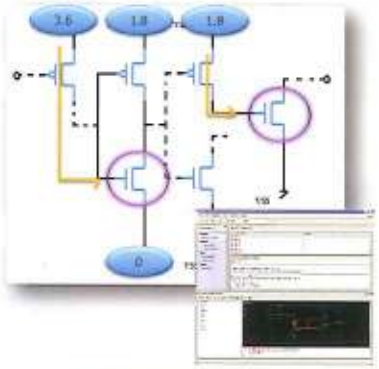


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Perform EOS Checking without Simulation
By Calibre PERC Voltage Propagation

- EOS has historically been one of the leading causes of integrated circuit failures, regardless of the semiconductor manufacturer
- The result of an EOS event can range from no damage or degradation to the IC up to catastrophic damage where the IC is permanently non-functional

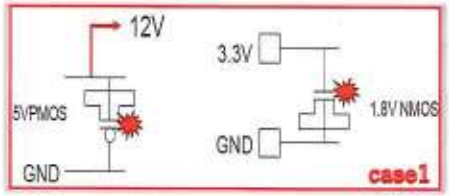


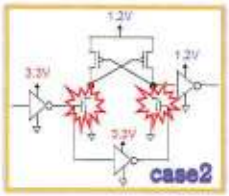


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Electrical Over Stress Check
Has been established In TSMC AMS REF 2.0 Reliability-Kit

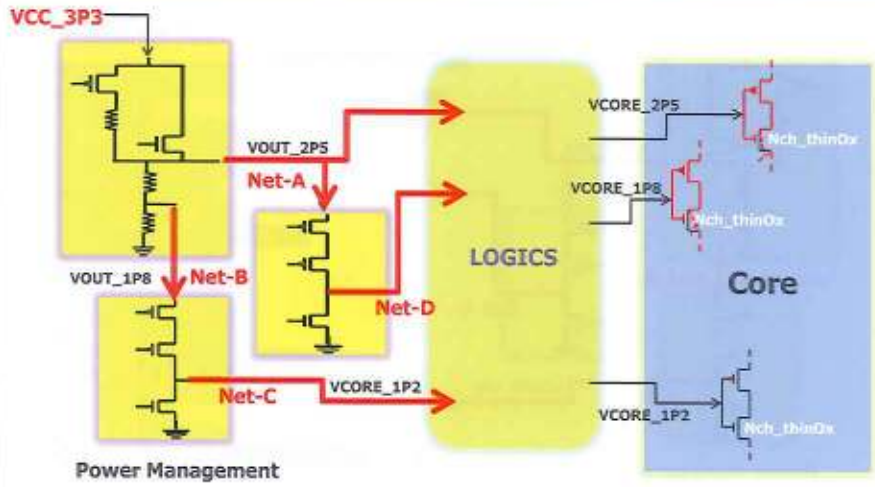
- LV device connected to HV power domain
 - Case1 : LV mos capacitor connected to HV power domain
 - Case2 : LV mos gate of level shifter connected to an output pin of HV power domain inverter





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PERC Traverse/Shift Voltage Across Circuits
Thin oxide gate stressed by high voltage can be detected



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Voltage Dependent DRC Become Very Critical Check For 20nm And Below Tech Nodes

- The thin dielectric between different node is under substantial electrical stress, and is prone to breakdown over time
- In foundry DRC, spacing criteria is raised when net is applied by higher than core voltage. The spacing criteria is further regulated into different level depending on voltage range of the net
- Foundry defines different marker layer for different metal layer to be recognized as different voltage range
- It is generally considered as user responsibility to place marker layer to layout net shapes

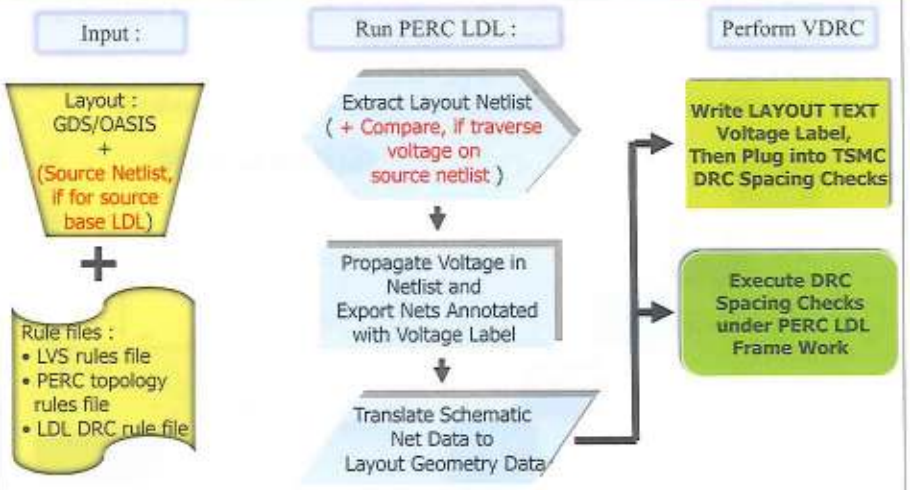
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Using Calibre PERC to Facilitate Voltage Dependent DRC

- Without right tool, it is very tedious to place right marker layers to the desired net polygons. If it is done in manual mode, it is error prone.
- It is seen as "not feasible" or "non robust" in real production design flow for generating voltage marker shapes through assistance of simulation tool.
- Calibre PERC provides an automatic way to propagate voltage into circuits and generate corresponding voltage label on geometry shapes

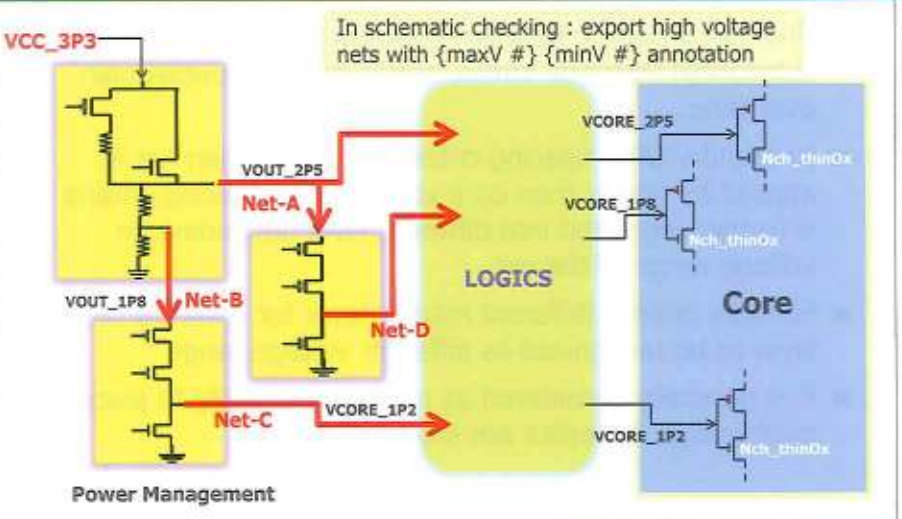
PERC Voltage Dependent DRC Flow

Voltage can be traversed on either source or layout netlist

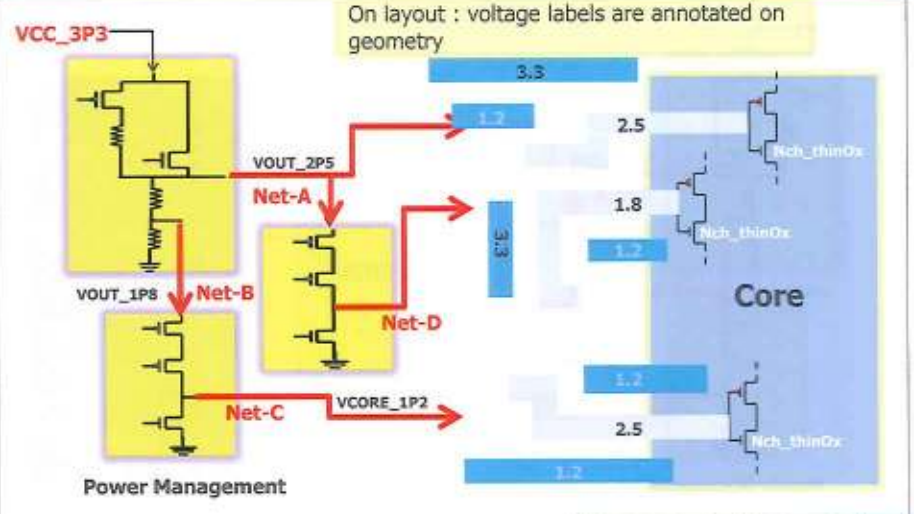


Apply Voltage Shift Constraint on Schematics

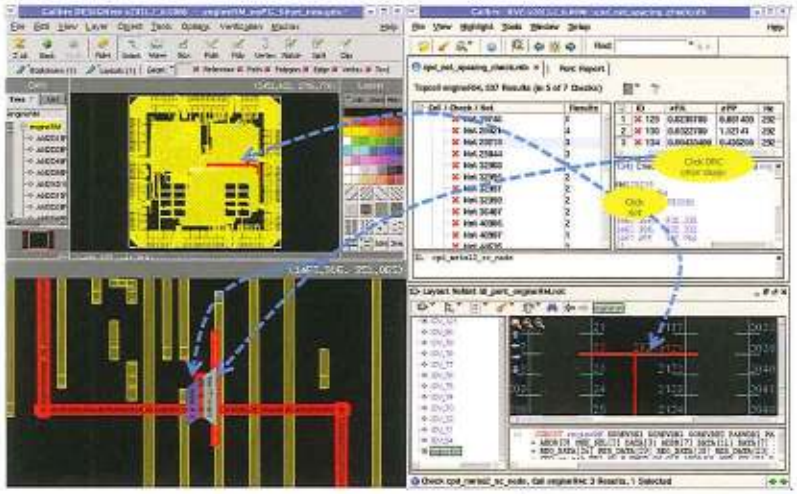
Generate appropriate voltage label inside core circuits



Voltage Labels are Annotated on Layout Geometry to Influence DRC Check Criteria



Debug PERC-LDL DRC By Using RVE



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Calibre PERC Strives for TSMC 20nmReliability Design Verification

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Modeling Voltage Variation in Physical Design with AOCV & POCV

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ABSTRACT

At smaller geometries modeling physical effects like process and voltage variation is an important part of a robust physical design flow. Today, designs are required to operate at multiple voltage corners, including near threshold voltage, and tolerate power supply noise.

It's important to consider these voltage requirements in all phases of the design. Timing derates can be used to addmarginto account for voltage and process variation to static timing analysis, for example. The choice of margin strategy can affect timing closure and yield. Systematic margining of these sources of variability is important. Over margining costs design time and QoR while under margining can risk the design or yield.

Both Advanced On-Chip-Variation (AOCV) and Parametric On-Chip-Variation (POCV) are used in physical design flows to model process variation today. These same techniques can be applied to model voltage variation effects without any change to existing physical design flows.

In this paper, we'll show how to incorporate both process and voltage variation in timing derates at the same time. We'll also demonstrate the impact of voltage variation on path delay for a variety of timing paths. Finally, we'll show how to examine the sensitivity of a library of cells to changes in voltage.

Modeling Voltage Variation in Physical Design with AOCV & POCV

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Director of Product Management
CLK Design Automation, Inc.

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WHY VOLTAGE VARIATION?

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Why model voltage variation?

Considerations

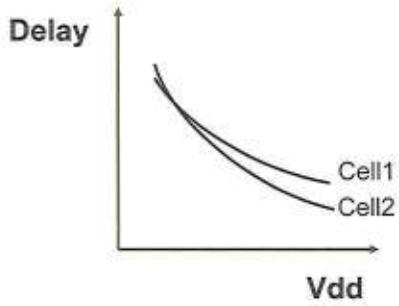
- ❑ Power supply noise
- ❑ IR drop
- ❑ Near threshold operation
- ❑ Sleep vs. active mode
- ❑ Multiple voltage corners

Desired Outcomes

- ❑ Improve STA results – closer to Monte Carlo SPICE
- ❑ Reduce over-design
- ❑ Reduce chance of missed violations
- ❑ Better cell behavior understanding

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Voltage Impact on Delay



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What is Voltage Variation?

- Small deviations in voltage along a path (power supply noise) that causes some cells to have shorter delays and others to have longer
- Two branches of a path see slightly different voltages due to different IR drop conditions causing timing differences across different branches
- Volatage induced delay effects are especially important in clock paths

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Low Power Design

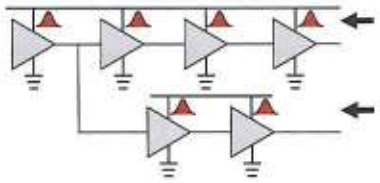
Designs require innovative electrical architectures, with multiple power domains and ability to run blocks at wide voltage range in order to meet performance and power specifications

- Over-drive, under-drive, near threshold operation
- Operational voltage can change on demand
- Operational voltage range for blocks much larger than previous designs

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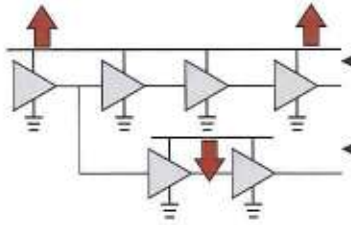
Modeling Voltage Variation

Power Supply Noise



Each cell has independent voltage

IR Drop



Higher fixed voltage for launch

Lower fixed voltage for capture

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AOCV & POCV

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AOCV & POCV

- AOCV & POCV can model process, voltage, and temperature on-chip-variation (OCV)
- AOCV & POCV are used in static timing analysis in the place of a global OCV de-rate factor
- **Both are useful for applying variation to static timing and optimization**
- Each has slightly different use models and limitations

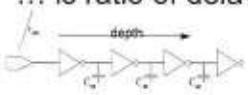
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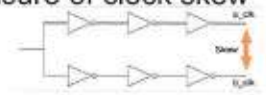
AOCV Primer

- AOCV de-rate is a function of cell, path depth, clock or data path, early or late analysis, and rise or fall arc

 de-rate = fn(cell, path depth, clock or data, early or late, rise or fall)

- … is ratio of delay or measure of clock skew





$$\frac{\mu_{delay} \pm (\sigma_{delay} * N_{sigma})}{CornerDelay} \qquad 1 \pm \frac{\sigma_{skew} * N_{sigma}}{CornerDelay}$$

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POCV Primer

- POCV coefficient is a function of cell, clock or data path, early or late analysis, and rise or fall arc

 coefficient = fn(cell, clock or data, early or late, rise or fall)

- Modeled as ratio of statistical contribution to delay over nominal statistical delay

$$\frac{\sigma_{delay}}{\mu_{delay}}$$

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How to Build AOCV & POCV Tables

- Simulate test structures (chains of cell under test) at characterized slew/load range
- Measure delays and derive de-rates or coefficients
- Requires simulation (often Monte Carlo SPICE or a dedicated tool like Variance FX)
- Use design rules or data mining to choose appropriate de-rate factors

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AOCV & POCV

- Both are big improvements over fixed OCV de-rate
- Both suffer from similar shortcoming – slew/load effects are missing from format
- **The Liberty Standards Group has approved the next Liberty modeling standard that will represent cell/arc/slew/load specific random variance (sigma) directly**

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MODELING VOLTAGE VARIATION WITH AOCV & POCV

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Define a Recipe

- Requires power analysis and design knowledge
- Do you want to model power supply noise, IR drop, or a combination of the two?
 - What's the worst case voltage difference for IR drop?
 - What's the N sigma voltage value for power supply noise?
- Do you want to combine voltage & process variation? (typically the answer is yes)?

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Comparison of Methods

Supply Noise

- Voltage and process variation combined as:

$$\sigma = \sqrt{\sigma^2_{voltage} + \sigma^2_{process}}$$

- Mean voltage at can be shifted to account for static IR drop
- For short paths may exaggerate effect of voltage variation values aren't chosen carefully

IR Drop

- Can model worst case power supply noise
- Requires statistical simulations at different voltages
- For long paths de-rate converges to ratio of delay for worst case noise over corner delay

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Limitations

- POCV format can only represent uncorrelated random variations
 - Works for power supply noise but can not represent correlated effects like IR drop
- Voltage variation requires a lot of simulation to capture delay variation for differing voltage
 - Consider advantages of special purpose tool vs. generic SPICE simulation + script

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VOLTAGE SENSITIVITY ANALYSIS

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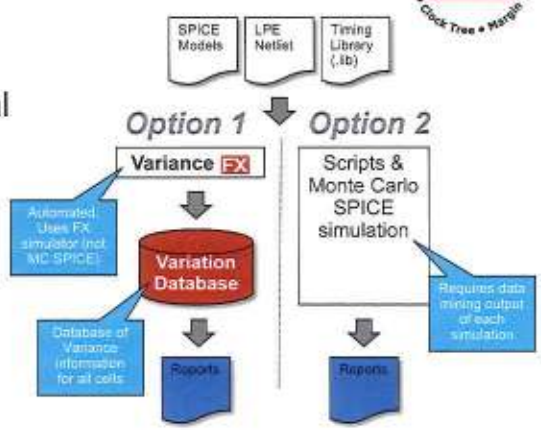
Voltage Sensitivity Analysis

- Depending on internal architecture, different cells' delays change differently to different supply voltages
- Rise/fall delays can also change differently to different supply voltages
 - Cells generally designed for symmetrical delays at nominal operational voltage
 - At lowered voltages delays can be highly asymmetric
 - Affects clock pulse widths etc.

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Methodology

Analyzes nominal delay and statistical delay variation, at given voltages, across all cells, all arcs, all loads, all slews of the given library

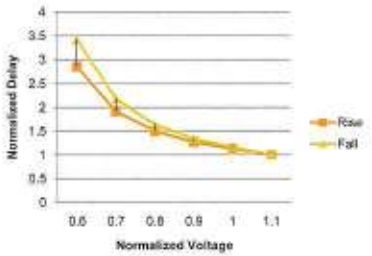


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Data Analysis

- Look for cells with asymmetry
- Look for cells with different profiles in the same family

Rise and fall inverter arcs analyzed between +10% and - 40% of nominal voltage



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Summary

- Modeling power supply noise and IR drop is important for low power designs and at advanced process nodes
- AOCV & POCV are useful tools for adding voltage variation analysis to existing physical design flows
- Voltage sensitivity analysis helps with architectural decisions early in the design process
- **All of these technologies are available and used in production environments today**
- More information at www.clkda.com

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Avoiding Cell Time in Monte Carlo: High-Sigma Standard Cell Optimization

Solido Design Automation

TSMC 2013
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ABSTRACT

This paper presents afast, industrial-scale approach to design and verify standard cells with SPICE accuracy at 4, 5, and 6 sigma, which is being used by leading design teams on advanced TSMC nodes. One previous approach was to optimize standard cells at PVT corners, which ignores local variation and has an inadequate model of global variation at modern TSMC process nodes. Another previous approach was to use ≈1000 Monte Carlo samples in the optimization loop, but that is extremely simulation-intensive and only has accuracy to 3-sigma. Other approaches assume Gaussian or unimodal distributions, which compromises accuracy. This paper presents a solution that, unlike previous approaches, is simultaneously fast, accurate, scalable, and verifiable. It combines a fast high-sigma analysis tool with a fast global optimizer (Solido High-Sigma Monte Carlo, and CellOpt). The analysis tool extracts high-sigma corners; the global optimizer sizes against the corners; and finally the analysis tool performs high-sigma verification. The tools use SPICE in the loop, but leverage adaptive data-mining techniques to quickly identify the points in design & process space to simulate. The tools account for local & global process variations, environmental variations, parasitics, and more. This paper will present industrial results, showing how the approach reduces power, lowers area, and reduces delay (all in a high-sigma sense) on individual cells and across whole cell libraries.

Avoiding Cell Time in Monte Carlo: High-Sigma Standard Cell Optimization

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trentmc@solidodesign.com

TSMC OIP Symposium
October, 2013

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Outline

- Problem Overview
- Previous High-Sigma Analysis Approaches
- Solido High-Sigma Monte Carlo (HSMC)
- High-Sigma Standard Cell Optimization

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The Problem

- Designing and maintaining standard cell libraries is expensive
 - Lots of simulator licenses
 - Lots of design time
 - High relative cost to achieve top competitive quality
 - Variability makes it difficult to size cells optimally
- Maintaining standard cell libraries includes:
 - Tuning, Porting, Retargeting, Migration, ...
- Only getting worse at smaller technologies

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Key Challenges

1. Statistical analysis is slow and inaccurate
 - High-sigma analysis needs too many Monte Carlo samples
 - No reliable way to get the full-sigma distribution
2. Library optimization is expensive
 - Expensive to do manually
 - Existing automatic solutions are not well-suited:
 - Too heavyweight (setup, constraints, large # of simulations)
 - Not tuned specifically for standard cells
 - Restricted to specific simulators
 - Not command-line friendly
 - Not variation-aware

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Outline

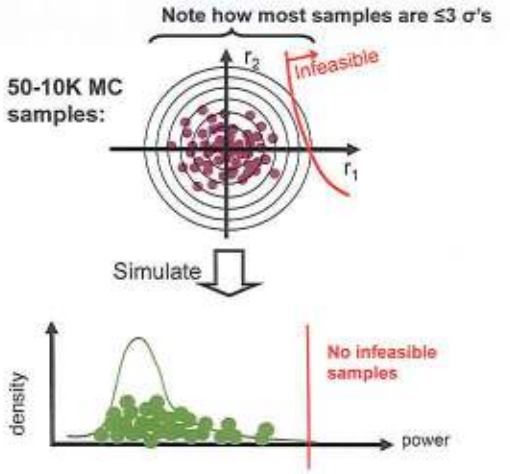
- Problem overview
- Previous High-Sigma Analysis Approaches
- Solido High-Sigma Monte Carlo (HSMC)
- High-Sigma Standard Cell Optimization

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solido

Approach: 10K Monte Carlo Samples

	10K Monte Carlo Samples
Fast	Yes
Accurate	**No**
Scalable	Yes
Verifiable	Yes

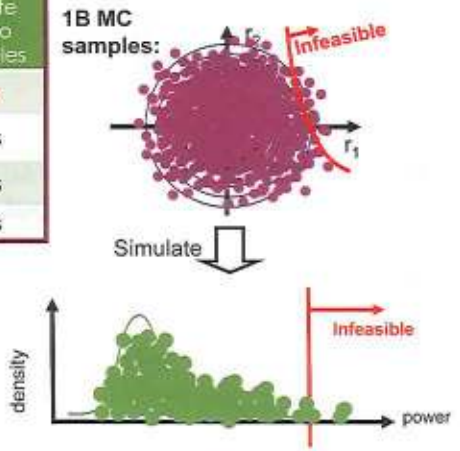


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Approach: 1B Monte Carlo Samples

	10K Monte Carlo Samples	1 Billion Monte Carlo Samples
Fast	Yes	**No**
Accurate	**No**	Yes
Scalable	Yes	Yes
Verifiable	Yes	Yes

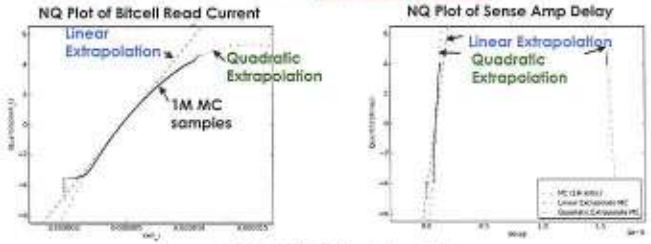


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Approach: Monte Carlo + Extrapolation

	10K Monte Carlo Samples	1 Billion Monte Carlo Samples	20K+ Monte Carlo Samples + Extrapolation
Fast	Yes	**No**	Yes
Accurate	**No**	Yes	**No**
Scalable	Yes	Yes	Yes
Verifiable	Yes	Yes	**No**



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Approach: Importance Sampling (IS)

	10K MC Samples	1B MC Samples	1M MC Samples + Extrap.	Importance Sampling **Local \| Global**
Fast	Yes	**No**	**No**	Yes \| **No**
Accurate	**No**	Yes	**No**	**No** \| Yes
Scalable	Yes	Yes	Yes	Yes \| **No**
Verifiable	Yes	Yes	**No**	**No** \| **No**

Problems:
- How to find most probable failure region(s)?
 - Local optimize: gets stuck in local optima → optimistic yield estimate, expensive on large circuits.
 - Global optimize: exponentially expensive
- How to capture whole feasible-infeasible boundary? A challenge when a broad region is (nearly) equally probable
- Messes with distribution
- **Does not answer: Can I trust it? Can I tell when it's inaccurate?**

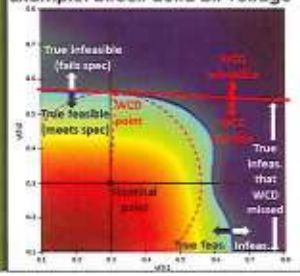
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Approach: Worst-Case Distance (WCD)

	10K MC	1B MC	1M MC + Extrap.	Importance Sampling **Local \| Global**	Worst-Case Distance **Local \| Global**
Fast	Yes	**No**	**No**	Yes \| **No**	Yes \| **No**
Accurate	**No**	Yes	**No**	**No** \| Yes	**No** \| Yes
Scalable	Yes	Yes	Yes	Yes \| **No**	Yes \| **No**
Verifiable	Yes	Yes	**No**	**No** \| **No**	**No** \| **No**

Example: bitcell delta bit voltage



Problems:
- How to find most probable failure point(s)?
 - Local optimize: gets stuck in local optima, expensive on large circuits.
 - Global optimize: exponentially expensive
- How to compute feasible-infeasible boundary?
 - Assume linear?
 - Quadratic? Expensive...
- (Usually) assumes a single failure region
- **Does not answer: Can I trust it? Can I tell when it's inaccurate?**

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Outline

- Problem overview
- Previous High-Sigma Analysis Approaches
- Solido High-Sigma Monte Carlo (HSMC)
- High-Sigma Standard Cell Optimization

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Rethinking the High-Sigma Problem

Hint: Benefit of Monte Carlo: computational complexity is *independent of dimensionality* (pretty amazing!)

Hint: In other domains, can simplify the problem by adding more information about the problem

Hint: Saying "problem is 6 sigma" is (just) 10^{10} MC samples. $10^{10} \ll 10^{150}$

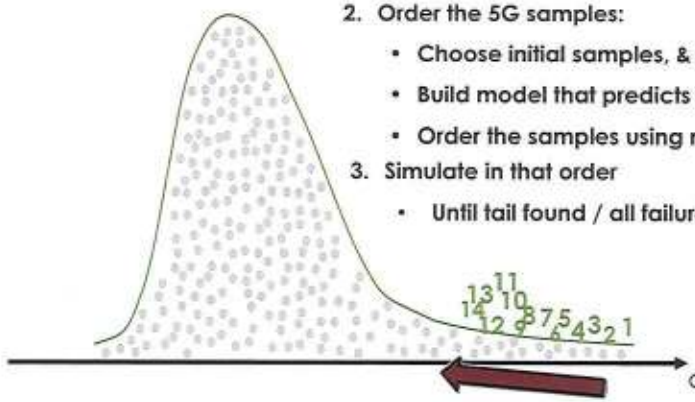
(10^{150} is size of sense amp delay's search space if 10 values per variable)

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Solido High-Sigma Monte Carlo (HSMC) Algorithm

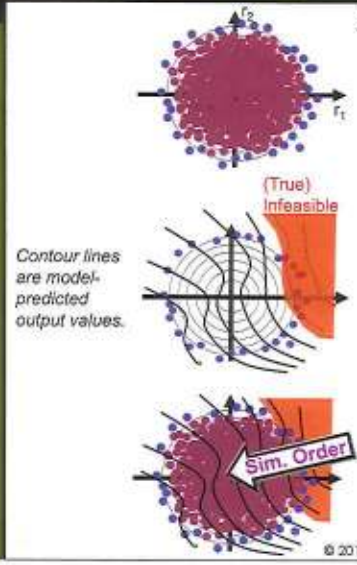
1. Generate (but don't simulate) 5G Monte Carlo samples
2. Order the 5G samples:
 - Choose initial samples, & simulate
 - Build model that predicts order
 - Order the samples using model
3. Simulate in that order
 - Until tail found / all failures found



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Solido HSMC Algorithm (Detailed)



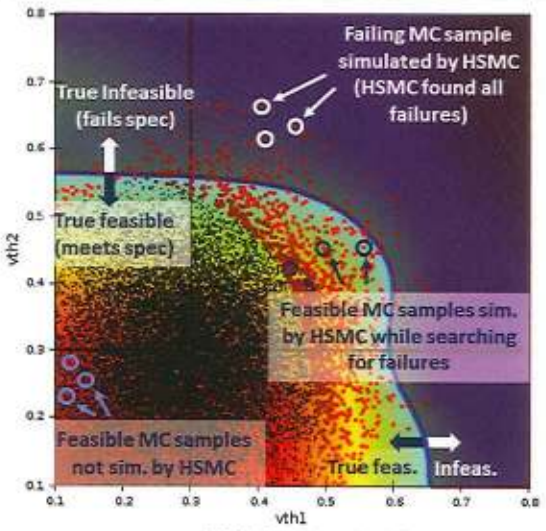
HSMC Algorithm:

- Generate (but don't simulate) 1B Monte Carlo samples.
- Choose initial samples = the 1000 generated samples that are farthest from nominal.
- Simulate initial samples.
- Build model that predicts order, mapping process points → simulated output values.
- Order the samples using model. Simulate the points in order, until all failures found or max # sims hit.

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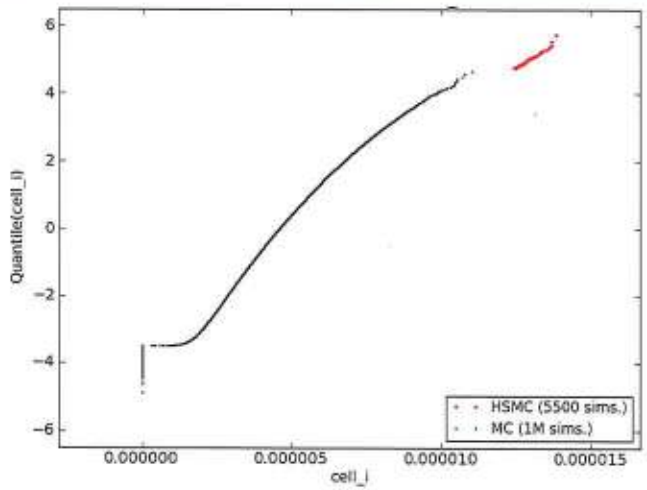
Solido HSMC on Bitcell Delta Bit Voltage



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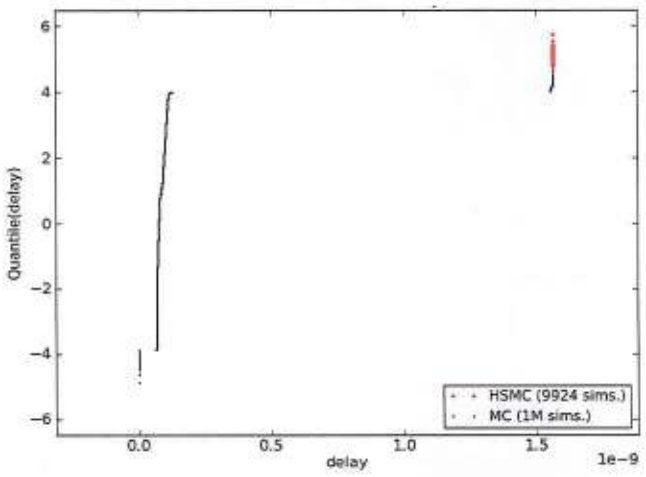
Solido HSMC in Action: NQ Plot of Bitcell cell_i



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Solido HSMC in action: NQ Plot of Sense Amp Delay



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Verifiability of Solido HSMC

A "Verifiable" tool addresses the user questions:

- **How can I trust it?**
- **If it fails, how can I tell?**

Example: when SPICE is doing poorly, its KCL-solving convergence does not go to zero, and it says so

The "KCL solve" in Solido HSMC is the output vs. sample convergence plot

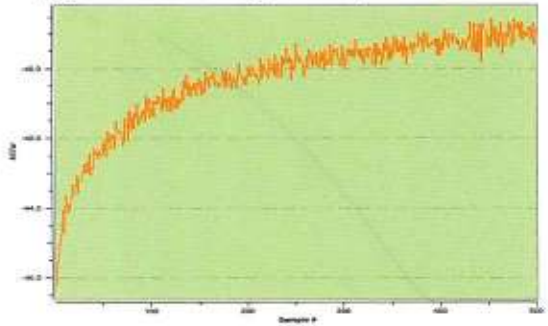
- Shows how well Solido HSMC ordered the samples
- If the convergence plot has a **trend away from the most extreme samples**, then Solido HSMC is working
- The convergence plot will always have some noise; this is perfectly normal

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Verifiability of Solido HSMC: When HSMC is Working Well…

- A very good convergence plot looks like this:



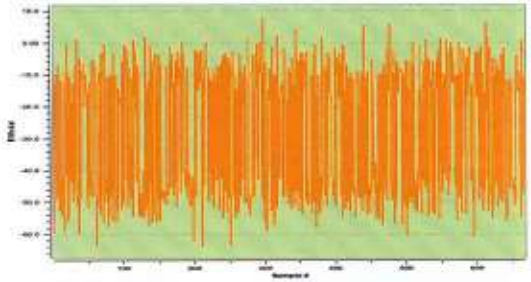
- HSMC has ordered the samples very well, so it has converged quickly

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Verifiability of Solido HSMC: When HSMC Doesn't Converge…

- It's easy to see when HSMC doesn't converge!
- The plot will look like this



- Various user actions available. Most common is to investigate issues in test bench/output measure set-up

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Comparison: Solido HSMC

	10K MC	1B MC	1M MC + Extrap.	Importance Sampling **Local \| Global**	Worst-Case Distance **Local \| Global**	**HSMC**
Fast	Yes	**No**	**No**	Yes \| **No**	Yes \| **No**	**Yes**
Accurate	**No**	Yes	**No**	**No** \| Yes	**No** \| Yes	**Yes**
Scalable	Yes	Yes	Yes	Yes \| **No**	Yes \| **No**	**Yes**
Verifiable	Yes	Yes	**No**	**No** \| **No**	**No** \| **No**	**Yes**

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Solido HSMC: Key attributes

- **Fast**
 - Typically consumes <5000 simulations; often <1000
 - Simulations parallelize on a cluster
 - Overhead is minutes to hours, depending on # samples, # process variables, and # cluster nodes
- **Accurate**
 - Monte Carlo accurate up to true 6 sigma (5G-10G samples)
 - SPICE accurate in tails
- **Scalable**
 - Handles tens, hundreds and even thousands of process variables
 - Can verify out to true 6 sigma with Monte Carlo and SPICE accuracy
- **Verifiable**
 - Output vs. sample convergence curve reveals accuracy in tails
 - Provides answers to "can I trust it?" and "Can I tell when it's inaccurate?"

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Outline

- Problem overview
- Previous High-Sigma Analysis Approaches
- Solido High-Sigma Monte Carlo (HSMC)
- High-Sigma Standard Cell Optimization

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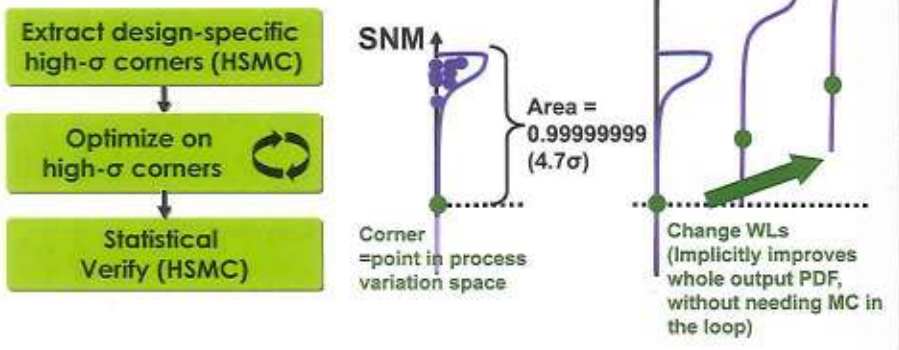
Challenges in Standard Cell Sizing

- Designing and maintaining standard cell libraries is expensive
 - Many simulator licenses
 - Lots of design time (manual or automated – both pain)
 - Variability issues. Only handle PVT, not 4-5 sigma.
- Maintaining standard cell libraries includes:
 - Tuning, Porting, Retargeting, Migration, …
- Only getting worse at smaller technologies

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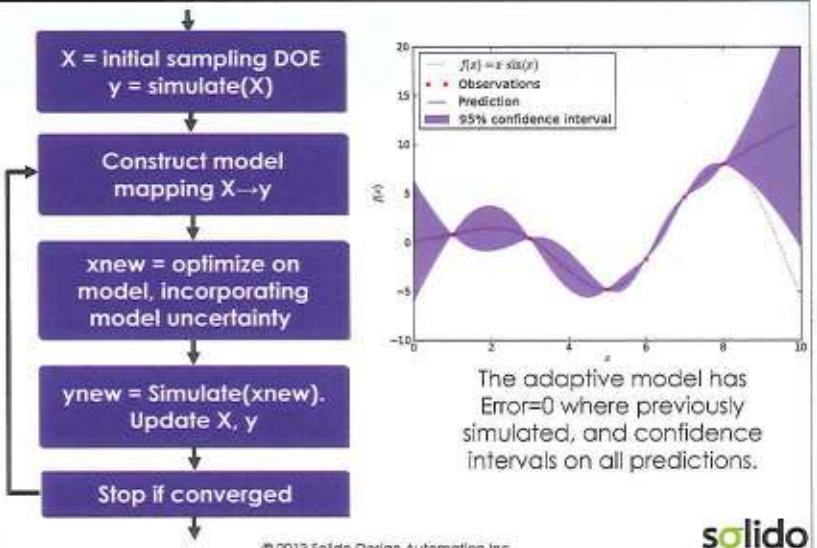
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Idea: Extract High-σ Corners (with HSMC), Then Automatically *Optimize on Them*



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Solido Cell Optimizer Uses Adaptive Modeling for Speed, Accuracy, Scalability and High-Quality Results



The adaptive model has Error=0 where previously simulated, and confidence intervals on all predictions.

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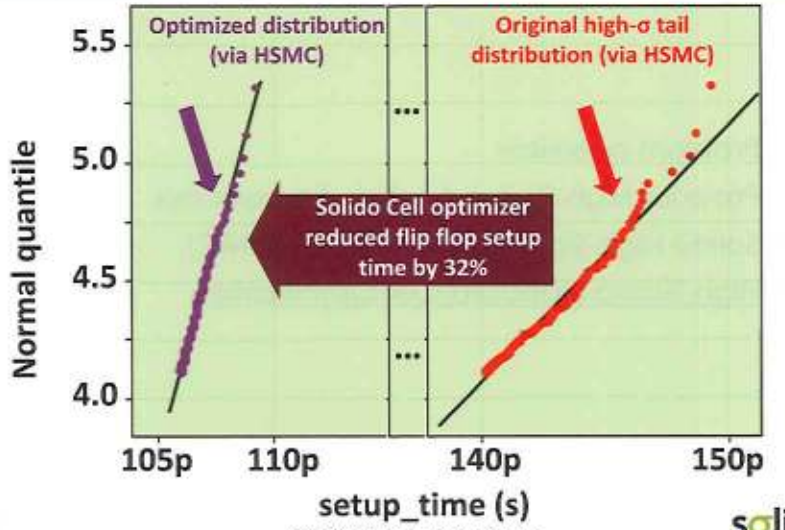
Solido Cell Optimizer - Example Results

Cell	# sims	Run time (min)	Overall Improvement (%)
DFF	355	15	20%
MBFF	512	30	19%
MUX	322	12	98%

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Solido High-Sigma Monte Carlo + Solido Cell Optimizer Enable High-σ Standard Cell Optimization

Example: minimize 5σ flip flop setup time



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Conclusion

- **Solido High-Sigma Monte Carlo (HSMC) enables fast, accurate, scalable, and verifiable analysis**
- **Solido Cell Optimizer uses HSMC high-σ corners**
- ***Enabling high-σ optimization of digital standard cells***



More detail:

T. McConaghy, K. Breen, J. Dyck, and A. Gupta. Variation-Aware Design of Custom Integrated Circuits: A Hands-on Field Guide. Springer, 2012.

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Inductive Component Compiler & IP Library

Helic

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

In recent years, accurate design of inductive components in advanced nodes that are compliant with demanding manufacturability rules is becoming more and more challenging. Using Helic's 20/16nm design technology, the process of preparing an IP library of ready-for-fabrication inductive components is simplified significantly thus slashing the time to production.

Helic's synthesis engine is easily configured according to the advanced node design guidelines to generate DRC-clean and DFM-correct inductive geometries, including single-ended, symmetrical spirals and sophisticated transformer devices. Helic's fast and accurate modeling engine uses techfile (iRCX, ITF) information to produce accurate broadband RLCk models.

The speed, ease of use and the Parameterized Spiral Synthesis capability of the Compiler enable the user to generate a complete library of spiral elements within an hour. The delivered library includes device layouts, models and a complete set of cellviews, such as schematics for LVS and symbols for simulation purposes. Moreover, the Compiler enables design closure by delivering corresponding iLVS compatible rules which are used in the physical verification flow.

Helic

Inductive Component Compiler & IP Library

-20/16nm

TSMC OIP Forum
October 2013



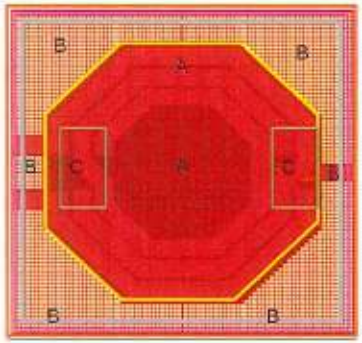
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Overview

- Problem: **Traditional spiral design methods fall short at 16/20 nm**
- Introducing Helic Inductive Component Compiler
- Setup/Input Requirements
- Design Example/Validation
- Summary

Helic 2

16/20nm DRC/DFM challenges



A, B areas

OD+POLY "fill" pattern

Mu, Mr, Mz, top Mx, ... M1 "drawing"

C = region of {[((Inter-VIAx AND INDDMY) SIZING 5 um)

M1+...+ top-2 Mx "drawing"

Helic 3

Dummy Tiles Specification - Example

- Region A (inside INDDMY):
- Chess like OD and POLY dummy tile pattern in fill purpose with width x length/spacing =1umx1um/1um and 0.9umx0.9um/1.1um → density ~25% and 20.25% in a 10x10 window resp.
- Mx dummy tiles in drawing purpose with minimum 1% density and 5% density for every three consecutive Mx:
 - For _4Mx: 1% den. in M5, M4, M2, and M1 (widthxlenght/spacing)=(0.5x0.5um/4.5um) and 5% den. in M3 (widthxlength/spacing)=(0.5x0.5um/1.5um) → density 6.25% in a 30x30um window
 - For _5Mx: 5% den. in M4 & M3 (widthxlength/spacing) =(0.5x0.5um/1.5um)
- Region B (outside INDDMY):
- Chess like OD and POLY dummy tile pattern in fill purpose with width x length/spacing =1umx1um/1um and 0.9umx0.9um/1.1um → density ~25% and 20.25% in a 10x10 window resp.
- M1 up to top Mx and Mr metal layers in drawing purpose with widthxlength/spacing =2umx2um/2um → density ~25%
- Mu metal layer in drawing purpose with widthxlength/spacing =3umx3um/3um → density ~25%
- Mx dummy tiles minimum spacing to boundary:dra is 0 um. Same for POLY and OD
- At least two rows of dummy tiles in the keep out area (especially for the minimum region B size)

Helic 4

Dummy Tiles Specification - Example

❑Region C (region of region of {[((Inter-VIA AND INDDMY) SIZING 5 um) SIZING -5 um) SIZING 5 um] AND INDDMY):

- Mx dummy tiles in drawing purpose in all the below Mx layers than the lower VIAx layer, below a VIAx+5um region that is inside INDDMY, with width x length/spacing=0.5umx0.5um/0.5um → density 25% for 10x10um window

-E.g. If Vx3 and Vx4 are the adopted inter via within (INDDMY SIZING 10 um) region, then the metal density within the check region for the M4, M3, M2 and M1 must be followed

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Traditional Methods Fall Short

- Traditional approaches to spiral design
 - Wait for foundry to provide "known good" instances
 - Design cycle time is of the order of 2 months per spiral
 - Long lead time for silicon correlation
 - Foundries taking longer and providing fewer geometries
 - Start with "known good" spiral geometry and adapt
 - Advanced DRC rules drive significant changes to the layout
 - Complex dummy fill requirements require weeks of manual layout effort
 - Final design no longer behaves like the "known good" spiral! – weeks of iterations required

Recent spiral inductor test chip design cycle ~4 months !!

Helic

Introducing Magic Wand

- User-controlled, ultra-flexible EM simulation driven synthesis engine
- Sophisticated library of spiral p-cells
- Correct by construction, fully DRC/DFM compliant

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User Specifies Requirements



Helic

Family of Solutions within Minutes!



- User selecst and instantiates any of the solutions
- Fully parameterized pcell along with all required views supports the entire design flow

Helic

Supports Multi-spiral Structures



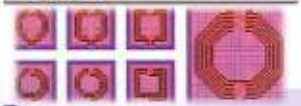


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Key Spiral CDF Parameters

Key parameters:

- ✓ Size X,Y
- ✓ Number of Turns
- ✓ Track width/distance
- ✓ Metal stack
- ✓ Bridge/C-Tap Width/Position/Type
- ✓ PGS option
- ✓ Dummy fill option
- ✓ Offset Temperature
- ✓ Tapering
- ✓ Non-45 sides length control
- ✓ Prim/Sec width/distance control
- ✓ Slotting





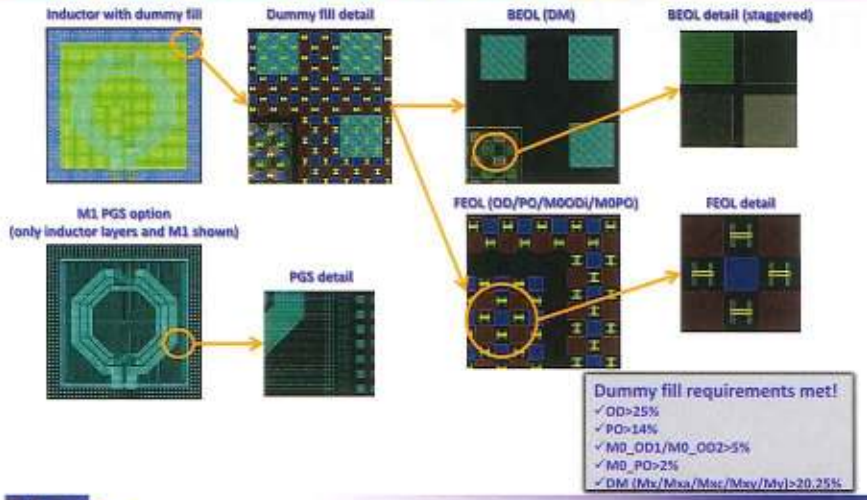
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Setup/Input Requirements

- BEOL stack electrical performance parameters
 - "Import" directly from iRCX files
 - Substrate parameters need to be added manually
 - Supports both "simple" and table based iRCX file formats
- Metal layer physical rules
 - Use built-in UI to enter min, max metal widths, via inclusion etc
- Tiling pattern definition via "tile file"

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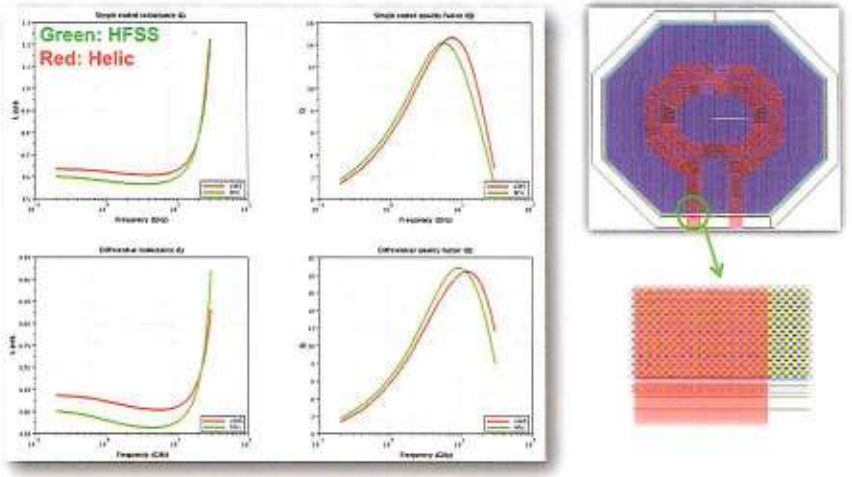
Helic Pcell Meets 16/20nm DFM Specs



Helic

13

Model Correlation with 3D EM @ 20nm



Helic

14

Summary

- Helic presents a flexible and fast inductor compiler that meets the complex DRC/DFM requirements of 16/20nm design
- Benefits include
 - Rapid generation of DRC/DFM clean inductor/balun pcells
 - Enables innovation through rapid iterations – generate a family of spirals with all required models and views within minutes!
 - Generate structures within a day of getting access to process information!
- Accuracy
 - Excellent correlation with customer golden reference data

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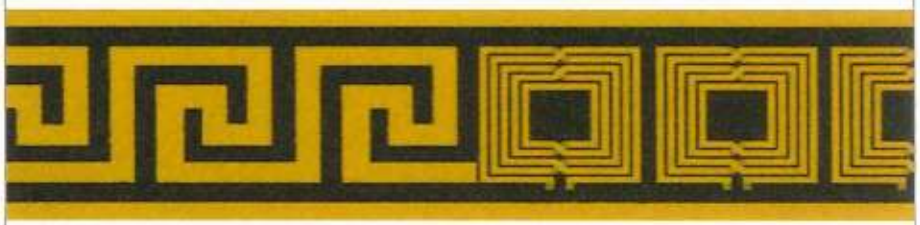
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Thank you!

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Break the tradition



ARM Implementation Solutions on TSMC Technologies for the Internet-of-Things

ARM

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

The increasing build out of the Cloud infrastructure and wireless connectivity has led to the proliferation of MCU-based embedded systems connected to the internet. This "Internet of Things" (IoT) leverages these embedded systems to gather information (e.g. sensors), locally process the data, and interact with other systems of the Cloud infrastructure. ARM will present its latest innovations in the Cortex-M series of microcontrollers, Artisan embedded memory, and low power standard cells that help designers achieve the power, performance and cost requirements of emerging IoT designs.

ARM Implementation Solutions on TSMC Technologies for the Internet-of-Things

Joel Rosenberg
Platform Marketing Director
TSMC OIP Forum 2013

Internet-of-Things Overview

Almost any imaginable product can now be connected to the Internet

- Enables new services, business models, improving efficiency and quality of life



Enabled by a confluence of existing technologies led by the ARM partnership

- Microcontrollers capable of efficient Internet connectivity, starting at under $1 and in 2mm^2
- Smart sensors, WiFi, Bluetooth, Zigbee, IEEE 802.15.4

ARM collaborates with partners to increase innovation opportunities

- ARM mbed is an industry standard, easy-to-use development platform

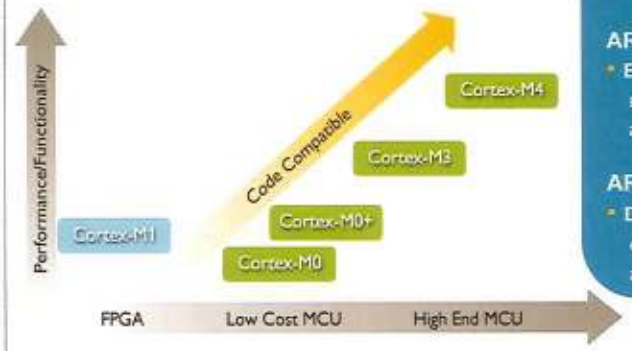
IOT-based SoC Challenges

- **More features at lower cost**
 - Increasing connectivity (e.g. USB, Ethernet, 802.15, NFC)
 - Higher control & data performance
 - Increased code drives need for embedded Flash on advanced nodes
 - Analog devices with increasing processing and communication
- **Energy efficiency (reduced active & static power)**
 - Wireless sensors, motor control, metering
 - Smaller batteries, energy harvesting
 - Wireless connectivity
- **8/16-bit running out of performance headroom**
 - As complexity rises so too do frequency and memory requirement
 - Increased performance with limited power budget



Cortex-M processor family

- **Seamless embedded architecture**
 - Spanning cost and performance points



ARM Cortex-A Series
- Applications processors for feature-rich OS and user applications

ARM Cortex-R Series
- Embedded processors for real-time signal processing and control applications

ARM Cortex-M Series
- Deeply embedded processors optimized for microcontroller and low-power applications

Microcontrollers Address Broad IOT Markets

Diverse Implementation (PPA) Requirements

Motor control
- ❑ Field oriented control
- ❑ Stepper motors
- ❑ BLDC motors etc

Connectivity
- ❑ Bluetooth
- ❑ Zigbee
- ❑ Ethernet, WIFI

Audio
- ❑ MP3 players
- ❑ Wireless headsets
- ❑ Virtual surround

Smart Metering
- ❑ Gas and water
- ❑ Electricity
- ❑ Connectivity

Power management
- ❑ UPS
- ❑ Lighting systems
- ❑ AC/DC converters

Human interfaces
- ❑ EPOS terminals
- ❑ Image processing
- ❑ Audio interfaces

Industrial Applications
- ❑ Appliances
- ❑ Lighting
- ❑ Motion control

Medical instrumentation
- ❑ Blood pressure meters
- ❑ Glucose meters
- ❑ Defibrillators

Automotive
- ❑ ABS systems
- ❑ Chassis control
- ❑ Airbag systems

Artisan Advanced Physical IP by ARM — The Architecture for the Digital World® ARM

Artisan Implementation Solutions for Embedded Processors

Ultra Low Power

Cortex™-M0+

Leakage optimized platforms
- Ultra-Low Power standard cells w/PMKs
- TGO libraries
- Ultra-low power memories

TSMC 90ULL
TSMC 110LP/LVP
TSMC 180ULL

Low Cost

Cortex™-M0

Area optimized platforms
- Ultra-high density standard cells
- High density memories

TSMC 90LP
TSMC 130G/BCD
TSMC 180G/BCD/MS/HV

Performance

Cortex™-M3/M4

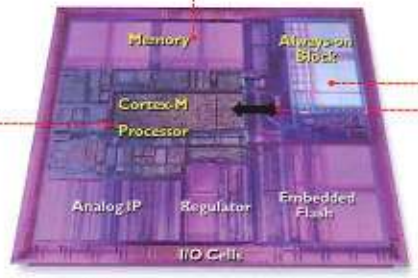
Performance optimized platforms
- High density standard cells
- High speed memories
- Ultra-low power memories + Logic

TSMC 40/55/65LP
TSMC 90G
TSMC 110G

Artisan Advanced Physical IP by ARM — The Architecture for the Digital World® ARM

Artisan Solutions for Embedded MCU Implementation

- Implemented with SC7 Base Library & PMK
- Implemented with SP-SRAM & SP Register File Compilers
- Implemented with Thick-Gate Oxide Library, PMK, LSK
- Base Library to implement processor with minimum leakage
- Multiple new power modes to reduce leakage
- TGO Library to Implement always-on functionality with minimum leakage
- PMK to implement DVFS, retention mode& clock gating
- Write-Assist Support for UD operation
- TGO PMK/LSK to implement level shifting & isolation



Typical Mixed-Signal SOC

Artisan Advanced Physical IP by ARM — The Architecture for the Digital World® ARM

DesignStart™ Starting Point for Customer Evaluations

Online Access to ARM IP



Over 8,000 products:
- **Physical & Processor IP**
- **Robust product search and full design views**

http://designstart.arm.com

Artisan Advanced Physical IP by ARM — The Architecture for the Digital World® ARM

TSMC / ARM Artisan Partnership

TSMC and ARM commitment to providing industry leading implementation solutions from 250nm → 16nm and beyond

	16/nm FinFET	20nm	28nm	40nm	55nm	65nm	90nm	110nm	130nm	180nm	250nm
tsmc	I	I	I	I	I	I	I	I	I	I	I

Artisan
Advanced Physical IP by ARM

NOTE

Increasing SoC Memory Performance By an Order of Magnitude

Memoir Systems

TSMC 2013
Open Innovation Platform®
Ecosystem Forum



ABSTRACT

Embedded memory performance is limited by clock speed. Algorithmic Memory builds multiport memories by combing the power of algorithms, built on conventional embedded memory libraries. These ports can be accessed simultaneously and improve embedded memory performance by up to 10X. Mathematically proven and formally verified, the technology has been adopted in processing heavy applications such as high performance networking, SDN, data-centers and HD-video architectures, and can also be used in the design of several key blocks of a modern microprocessor, such as multiported L2/L3 tags, snoop tags, instruction and data caches, as well as specialized memories for Mobile, DSP, Cloud Processing and Graphics.

Algorithmic Memories also offer up to 60 % lower area and power, 30% higher clock frequency, reduced risk and memory development time, and help unlock the true potential of multicore, data-pipelined and parallel SoC memory architectures.

With algorithms that have been customized for memory libraries on TSMC's 40 nm and 28 nm process nodes, Algorithmic Memory enables designers to achieve optimal memory performance, power, and area. Further, by allowing designers to create new high performance, high capacity multiport memories based on TSMC's reliable physical memory, Algorithmic Memory enables them to develop high performance and highly reliable SoC architectures.

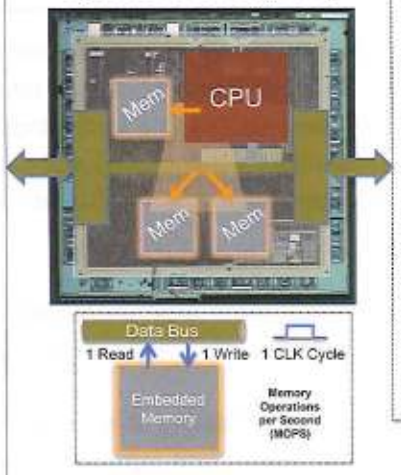
MEMOIR SYSTEMS

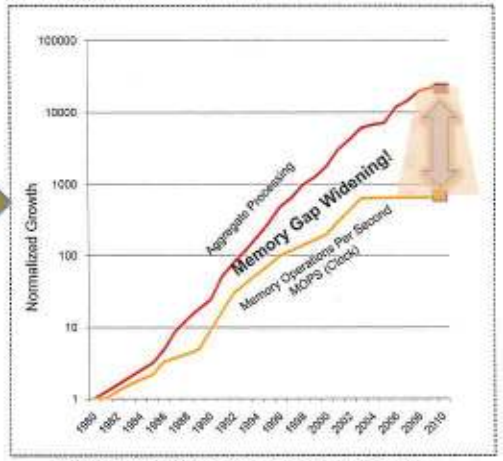
Increasing SoC Memory Performance By an Order of Magnitude

Sundar Iyer, Co-founder & CEO
sundaes@memoir-systems.com

Problem: The "Processor Memory" Gap….

System on Chip (SoC)



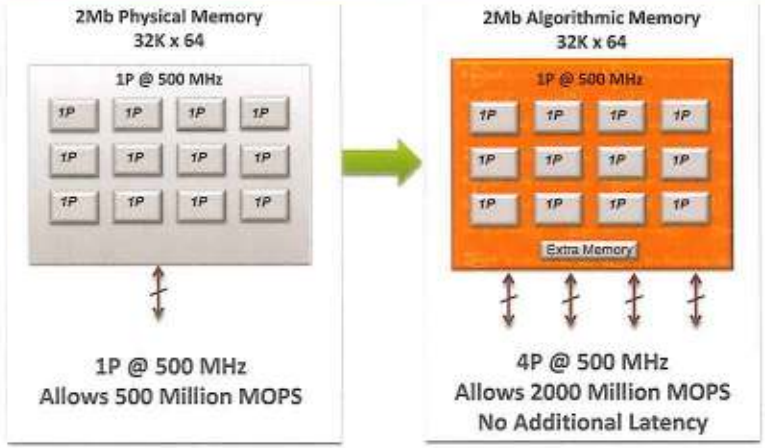


"Source: Hennessy Patterson, "Computer Architecture," 5th Edition

MOPS = Memory Operations Per Second
Measured as Random Access Transactions

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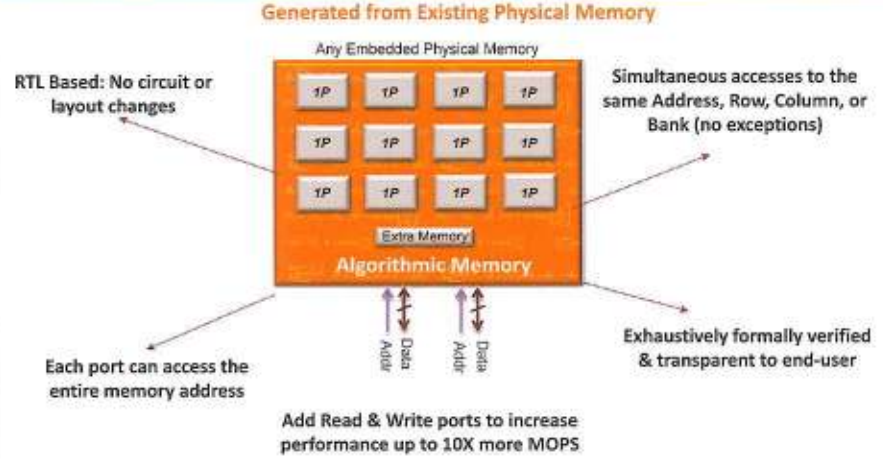
Solution: **Algorithmic Memory®= Memory Macros + Algorithms**



Before **After**

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Solution: Algorithmic Memory Technology



Using Existing Physical Memory to Build any Multiport Functionality

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Extend Multiport Physical Memory Performance



Built from Existing Embedded Memory

- Reduces cost, time to market
- Reduces risk to build physical compilers

Better Performance, Power and Area

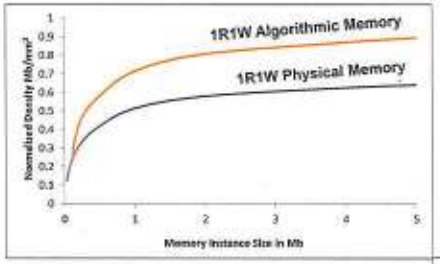
- Lowers area and power up to 60%
- Increases clock frequency up to 30%

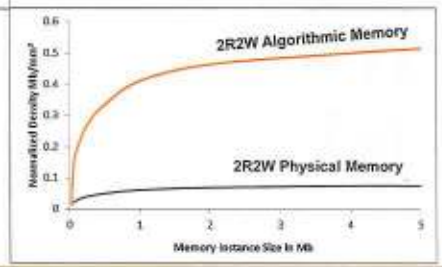
Integrates Seamlessly into ASIC Flows

- Exhaustively formally verified
- Supports standard SRAM interface
- Adds No additional clock cycle latency

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Reduces SoC Memory Area

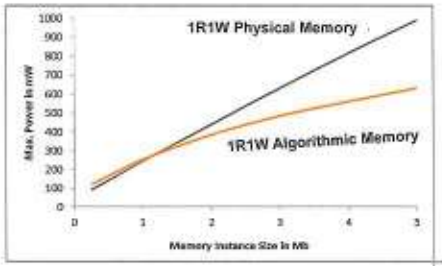


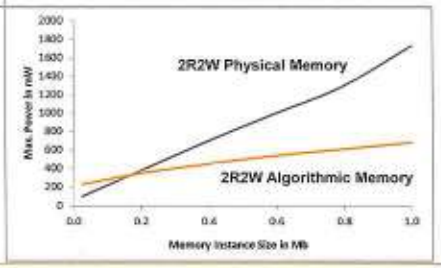


Normalized for 1P = 1 Mb/mm2

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Reduces SoC Memory Power





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Common Next Generation SoC Applications

Available on TSMC platform with >1GHz performance

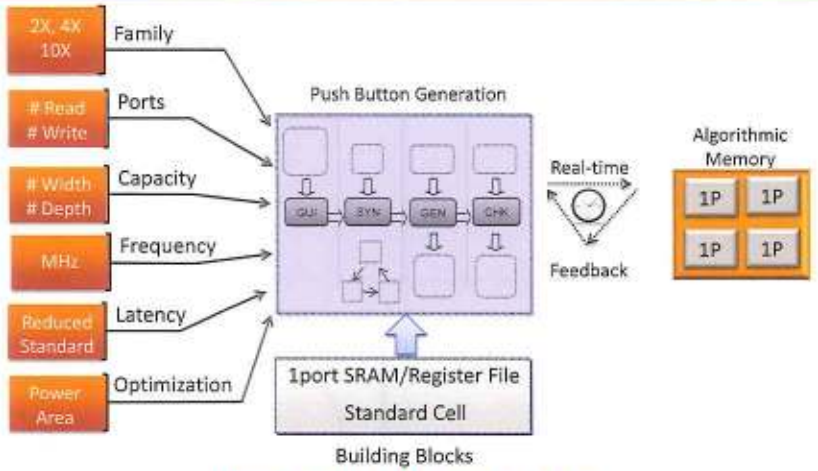


2X, 4X and 10X Multiport Families

- ***Data Communications: Networking/ SDN/Storage , Mobile Infrastructure/HPC***
 - Ingress buffers, egress buffers
 - Multicast descriptor lists
 - L2 MAC lookups, HPC lookups
 - Free lists for multicast buffers
 - Data and tag arrays for L2/L3 caches
 - Netflow, counters, state tables, linked lists
 - Route lookup tables
 - ACL tables
- ***HD Video***
 - Frame buffers
- ***High Performance Processors***
 - Multiprocessor L2/L3 tags/Caches
 - Mobile, application processor SoCs
 - DSP load/store units
 - Graphics SIMD register files
 - Video pixel structures

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Generate Memories in Real Time

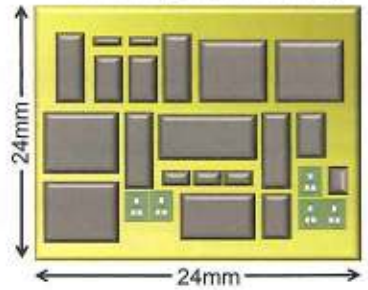


Memories up to 10 ports can be Generated on TSMC Platform in Real-time

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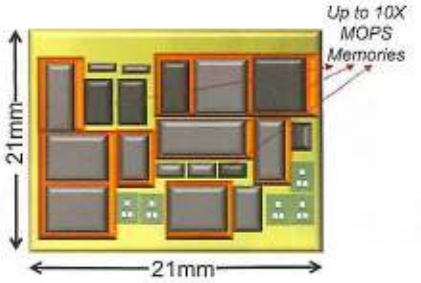
Power Performance and Area Benefits

Without Algorithmic Memory



- Area 576 mm²
 - 800 Mb of total memory
 - 165 memory instances
 - SRAM, RF, 2ports etc.
- Versatile memories required
 - 4R4W, 2R1W, 4W1R memories

With Algorithmic Memory



- Area 441 mm²
 - Area savings of 135 mm²
 - Decrease die size by 23%
 - 136 memory instances accelerated
- Power savings > 12W
- Up to 10X MOPS for select memories

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Improve the PPA Profile of Physical Memories

Algorithmic memories complement physical memories to...

1. Increase memory performance up to 10X
2. Increase memory ports up to 10X
3. Lower SoC area and power up to 60%
4. Increase multiport memory frequency up to 30%
5. Easily interface, integrate and implement
6. Reduce memory development time, cost & risk
7. Available now on TSMC advanced nodes

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NOTE

Beyond Soft IP Quality to Predictable Soft IP Reuse

Atrenta

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Open Innovation Platform®
Ecosystem Forum



ABSTRACT

Objective IP quality metrics are needed to support continued growth of the IP industry. Since 80% or more of every new chip is composed of 3rd party or legacy IP, the risks of using poorly developed IP are just too high. The industry needs an "IP quality vocabulary" to communicate completeness and quality of deliverables and subesequent integration risks.

Working with TSMC on their Soft IP Alliance, Atrenta and TSMC have jointly developed such a "vocabulary" using the Atrenta IP Kit and SpyGlass. The improvement in delivered quality for soft IP is demonstrable and TSMC's customers are reaping the benefits.

The work is not done however. Beyond known IP quality, users need more predictable ways to deploy reused IP – better implementation recipes, verification strategies and mutli-mode analysis are examples of what must come next. In this presentation, Atrenta will review the work done to date with TSMC and the results achieved. We will then look to the future and discuss methods to implement true soft IP signoff and advanced packaging methods to deliver the required materials to customers to address items such as functional verification and variability analysis.

SPYGLASS® FROM ATRENTA

Beyond Soft IP Quality to Predictable Soft IP Reuse

TSMC 2013 Open Innovation Platform® Ecosystem Forum – October 1, 2013

tsmc®
Open Innovation Platform®

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Agenda

SPYGLASS®

- **Soft IP Quality – Establishing a Baseline With TSMC**
- **Soft IP Quality – What We Checked and What We Found**
- **Soft IP Reuse – Methodology and RTL Signoff**
- **Summary and Next Steps**

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TSMC & Atrenta IP Kit History

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Atrenta Announces SpyGlass Tool Used in TSMC Soft IP Qualification Flow

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Quality reports generated by SpyGlass® to be available on TSMC web site

San Jose, Calif. and HSINCHU, Taiwan, R.O.C. — May 26, 2011 — Atrenta Inc. today announced the deployment of a comprehensive soft IP qualification program using Atrenta's SpyGlass® platform and a targeted subset of its G
qua
sem
TSM

Atrenta and TSMC IP Quality Initiative Gains Broad Industry Acceptance

SAN JOSE, Calif. - March 5, 2012 - Atrenta Inc., a leading provider of SoC Realization solutions for the semiconductor and electronic systems industries, today announced that 10 intellectual property (IP) providers have qualified their soft IP for inclusion in the TSMC 9000 IP library using the Atrenta IP Handoff Kit.

Atrenta and TSMC Announce SpyGlass® IP Kit 2.0 Availability

New soft IP qualification platform more comprehensive and easier to use

Digi
Inc.;
infor
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SAN JOSE, Calif and HSINCHU, Taiwan, R.O.C. — Oct 31, 2012 — Atrenta Inc., the leading provider of SoC Realization solutions for the semiconductor and consumer electronics industries, with TSMC announced today the planned availability of IP Kit 2.0.

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TSMC/Atrenta Collaboration

SPYGLASS®

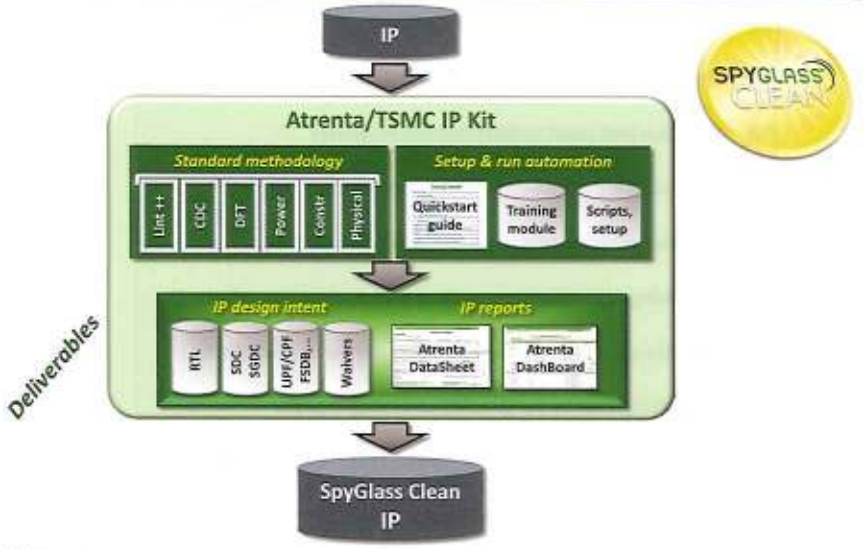
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- **Golden Rules for soft IP handoff analysis**
- **Definition of quality metrics to assess soft IP**
 - Modified severity of errors to conform to quality requirements
- **Enables various IP packaging types**
- **Optimizes work flow to ensure ease-of-use and reliable, fast operation**
 - Tuned mandatory vs. optional goals
- **Joint roll out plan development and beta testing with IP partners**
 - Ease of use a critical requirement

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IP Kit – Establishing IP Quality Baseline

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IP Dashboard Report

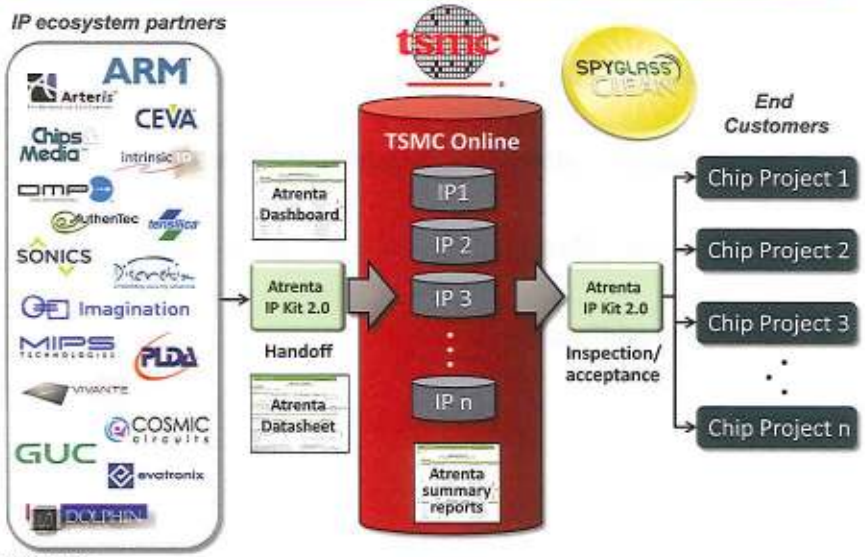
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TSMC Soft IP Qualification Program

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Strong Program Acceptance

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Agenda

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- Soft IP Quality – Establishing a Baseline With TSMC
- **Soft IP Quality – What We Checked and What We Found**
- Soft IP Reuse – Methodology and RTL Signoff
- Summary and Next Steps

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IP Kit – Sample Tests

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Power	What will the average power dissipation be?
	Are my power domains correctly defined?
Clocks & Timing	Are clock and reset constraints set properly?
	Are clock definitions consistent, correct and complete?
	Are clock domain crossing synchronizers bug-free?
	Are timing constraints consistent across block boundaries?
	Are false path and multi-cycle paths correctly identified?
Lint	Is the design ready for simulation and synthesis?
Test	What will the stuck-at and at-speed test coverage be?
	Can all sequential elements be scanned?

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What Did We Find?

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Many items that would impact integration/debug time and chip function were found & fixed

Some examples:

- Missing synchronizers on CDC paths causing possible chip function issues
- Data loss on fast-slow CDC paths
- Uncontrolled data path impacting transition fault coverage
- Index out of range which causes synthesizability issues
- Unconstrained I/O ports leading to poor SDC coverage

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TSMC customer benefit → *Faster time to silicon*

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Agenda

SPYGLASS

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Journey – Soft IP Quality to Soft IP Reuse

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- Soft IP quality is a necessary *but not a sufficient* condition for soft IP reuse
- Enforcing a known standard of quality for IP blocks is important
- How those blocks are assembled is just as important
- The concept of RTL Signoff* is a critical enabler for successful soft IP reuse



** RTL Signoff: A series of must-pass requirements before the flow proceeds*

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Traditional Signoff

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RTL → Synthesis → Layout → SIGNOFF → Fab



A series of must pass requirements before tape out

- Typically done post-layout
- Requires iterations with layout, synthesis and even RTL
- Design convergence becomes worse at 28→14 nm
- 3rd party IP's further increase the design risk
- Too late in the flow, too much design risk



Traditional signoff no longer sufficient

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RTL Signoff Emerges

SPYGLASS

RTL → RTL SIGNOFF → Synthesis → Layout → LAYOUT SIGNOFF → Fab



A series of must pass requirements before synthesis

- Does not replace, but augments post-layout signoff
- Minimize late stage surprises & iterations
- Must be applied to the entire design including 3rd party IP's
- Run times are an order of magnitude faster than post-layout

Only viable approach to address soft IP reuse

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RTL Signoff Requirements

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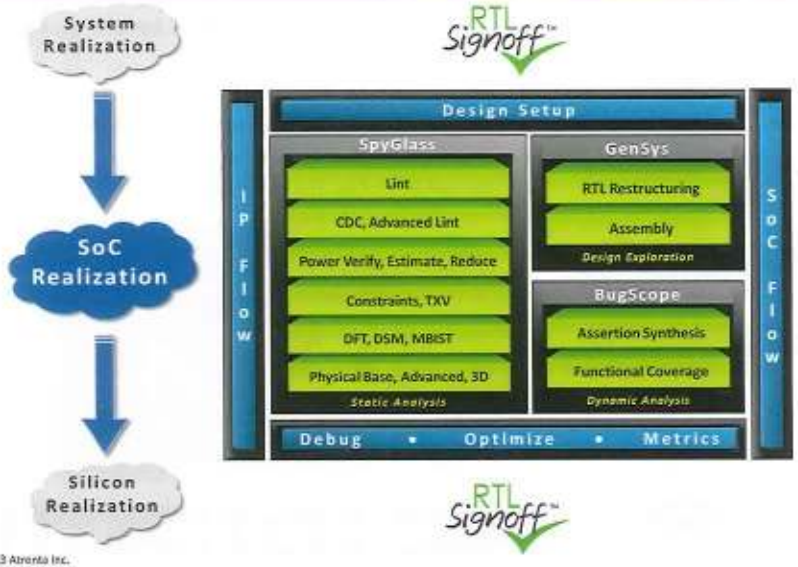
Signoff Domain	MUST PASS Requirements
Verification	✓ Functional coverage signoff ✓ High quality assertions checked into simulation regressions
CDC	✓ Clock, reset, data synchronization signoff ✓ Static (structural + formal), Dynamic (simulation) signoff
SDC	✓ Complete and consistent SDC to synthesis ✓ False & multi-cycle paths fully verified
Power intent (*PF)	✓ Power intent (UPF/CPF) signed off ✓ Must be done before & after insertion of level shifters, isolation logic, ...
Power	✓ Efficient clock gating for registers and memories ✓ RTL meets power spec - taking into account physical effects
Test	✓ RTL meets stuck-at test coverage requirements ✓ RTL meets at-speed test coverage requirements
Physical	✓ RTL is congestion-free, ✓ RTL meets area & timing targets

RTL Signoff applies to IP/blocks and full SoC

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Complete Platform for RTL Signoff

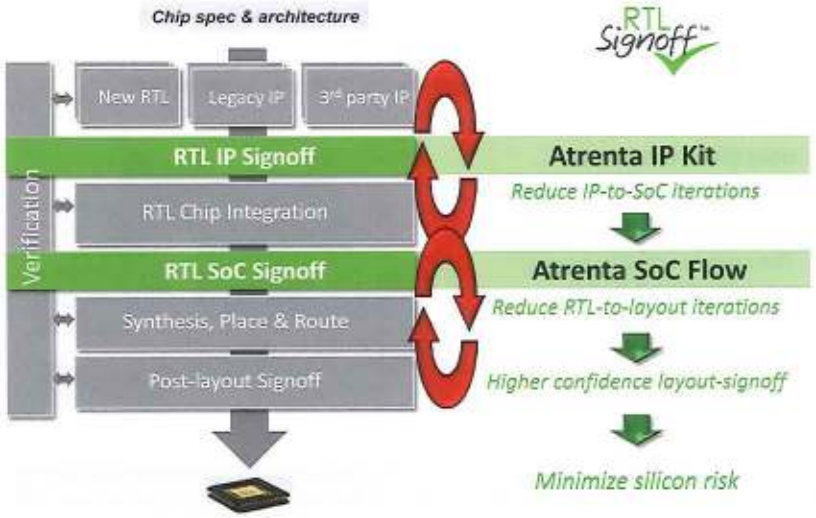
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RTL Signoff with Atrenta

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Agenda

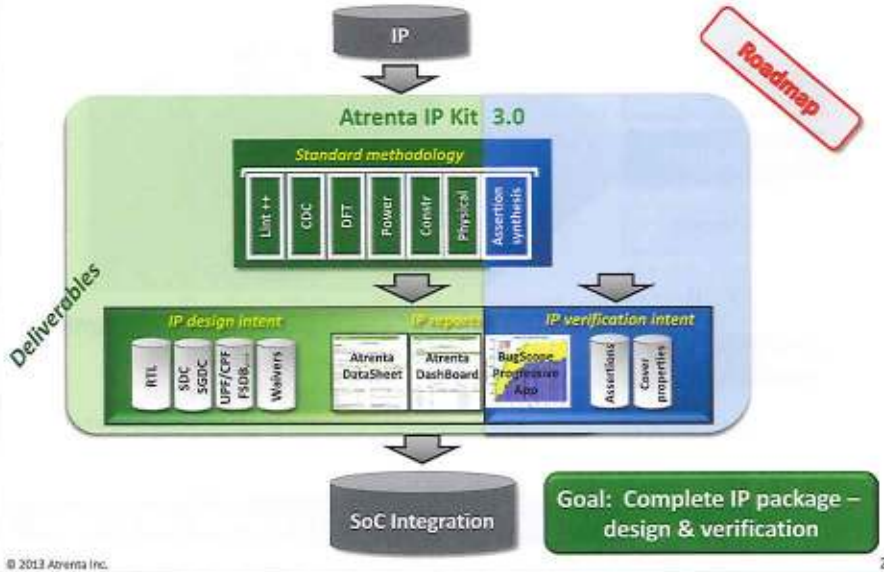
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- Soft IP Quality – Establishing a Baseline With TSMC
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Atrenta IP Kit 3.0 – Includes Verification

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Hierarchical SoC Abstraction Flow

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Design	Size [Gates]	# Blocks	Runtime [Hrs]		Memory GB		# Violations	
			Flat	Hier	Flat	Hier	Flat	Hier
Graphics chip	1.4 B	14	96	2	1300	100	> 1 M	346
Networking	155 M	12	20	0.5	300	30	6678	2
D-TV chip	110 M	26	33	1	400	50	1289	102
Mobile phone	100 M	9	8	0.5	200	40	1687	200

Billion+ gate capacity

15-50X faster

5-10X lower memory

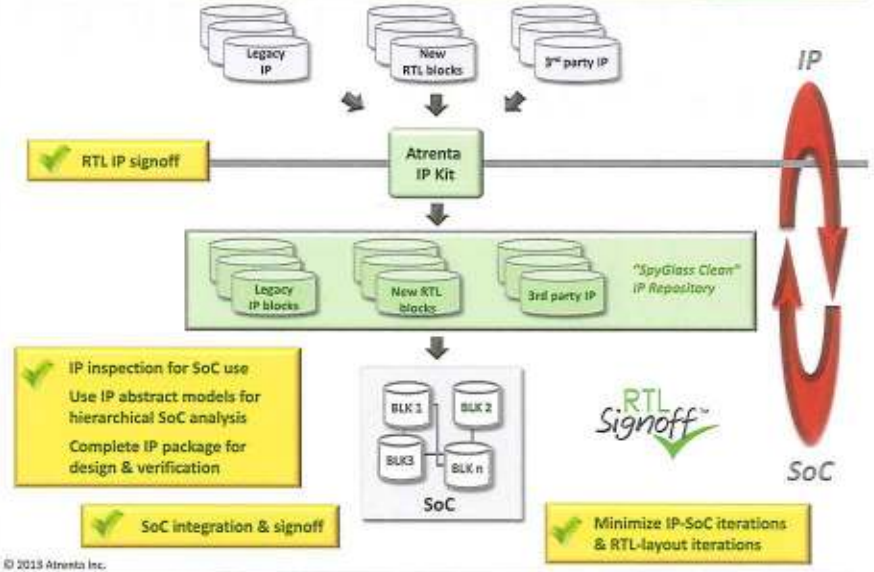
Goal: Manage Complexity

10-100X reduction in noise

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Soft IP Reuse – The Big Picture

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Thank you!

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OTP and MTP Logic Non-Volatile Memory Technologies Utilizing Charge-Trapping Mechanism

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ABSTRACT

A unique charge-trapping OTP memory technology has been developed in 0.18-um to 65-nm TSMC processes and passed TSMC's IP9000 qualification process. Low-voltage operations and small macro footprint have been achieved with a differential bit-cell and sense-amplifier architecture. Unlike conventional anti-fuse technologies readily available on the market today, every transistor and node in the charge-trapping OTP cell is testable without the need to program the bit cell. In addition to the OTP IP, we are developing MTP memory IP solutions that have up to 100K cycles of endurance.

The paper will present some of the targeted applications, technical requirements and technical details for these OTP and MTP technologies. The paper will also elaborate on how NSCore has cooperated with the TSMC IP qualification team through TSMC's IP9000 program, to ensure that the NSCore OTP IP meets the customers' high quality requirements.

The *hot-carrier effect* in semiconductor device physics is well known and has been deeply researched. Due to the indepth understanding of the behavior of the hot-carrier effect that has been gained over the last quarter century, the phenomena is a perfect vehicle for a NVM. The technology presented in this paper describes how the trapped charge from the hot-carrier effect is used to program and erase data in the bit cells of the OTP and MTP extremely reliably and predictably.

NSCore

OTP and MTP Logic Non-Volatile Memory Technologies Utilizing Charge-Trapping Mechanism

TSMC Open Innovation Platform
October 1, 2013

Kenji Noda
Executive VP & CTO
NSCore, Inc.

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Outlines

- Program and Read Mechanism
- OTP IP Lineup in TSMC Processes
- MTP Technology
- Application Examples
- Roadmap

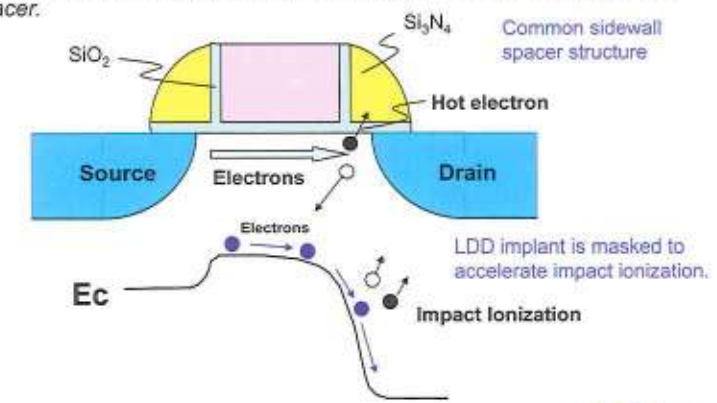
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Program and Read Mechanism for OTP

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Programming Mechanism

When nMOSFET turns ON, hot-electrons are generated and trapped in side-wall spacer.

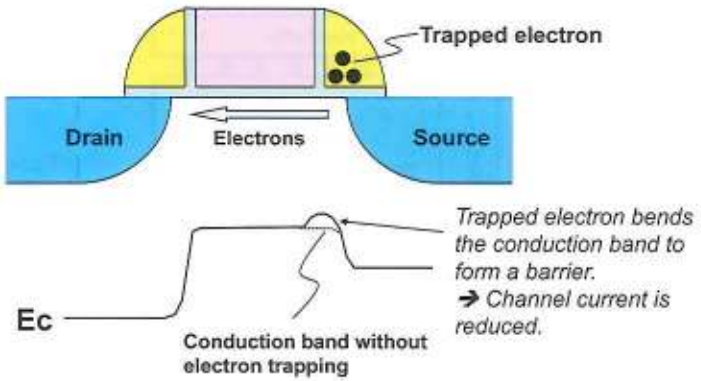


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In Read Operation

"Source" and "Drain" are reversed from Program Operation

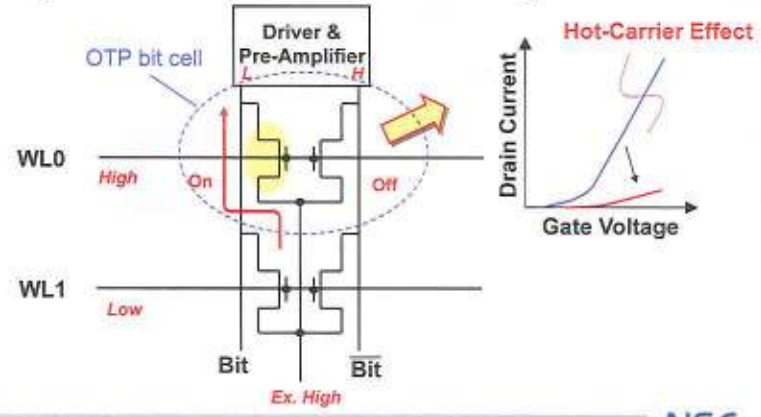


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Program Operation

Program current flows in one transistor in a cell and generate hot-carriers.

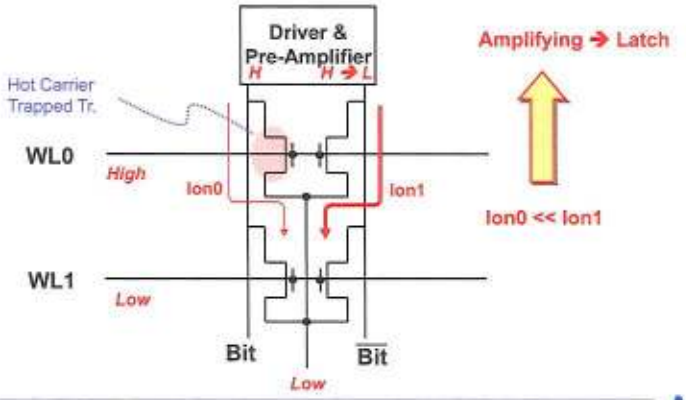


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Read Operation

Both bit-lines are pre-charged and current flows through selected cell transistors.
➔ Sense amplifier senses current difference and latches.



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OTP IP Lineup in TSMC Processes

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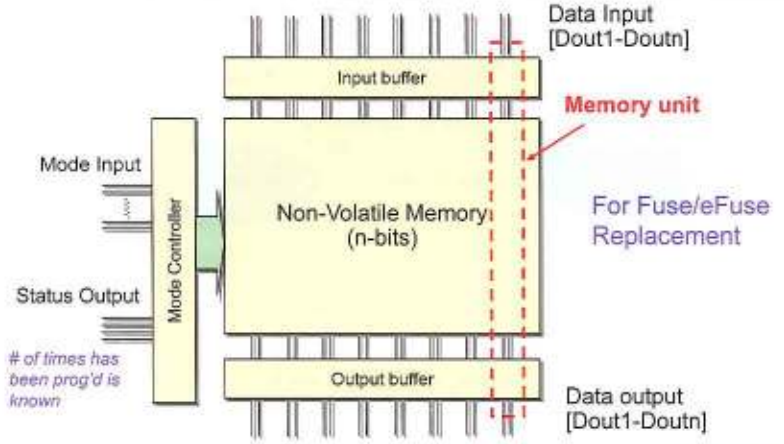
TSMC Processes Availability

✓TSMC 0.18μm	***IP9000 Full Qual.,*** Volume Production
✓TSMC 0.13μm	***IP9000 on-going,*** Volume Production
✓TSMC 0.11μm	Silicon Verified
✓TSMC 90nm	Silicon Verified
✓TSMC 65nm	***IP9000 Full Qual.,*** Volume Production

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Single-Word-line Architecture for Small Memory Size

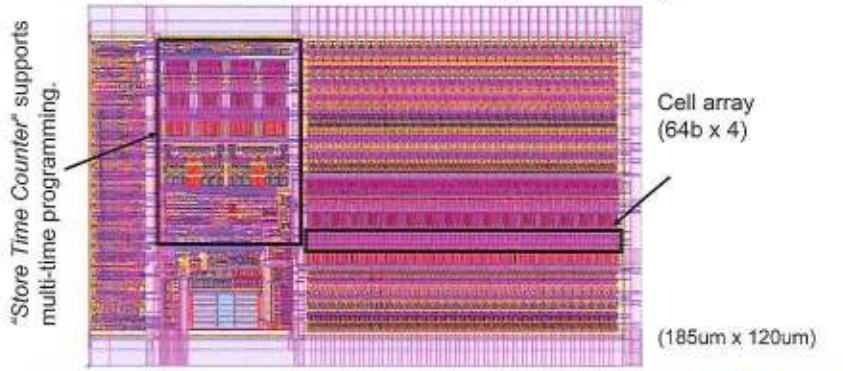


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256b OTP/64b 4-Time-Programmable

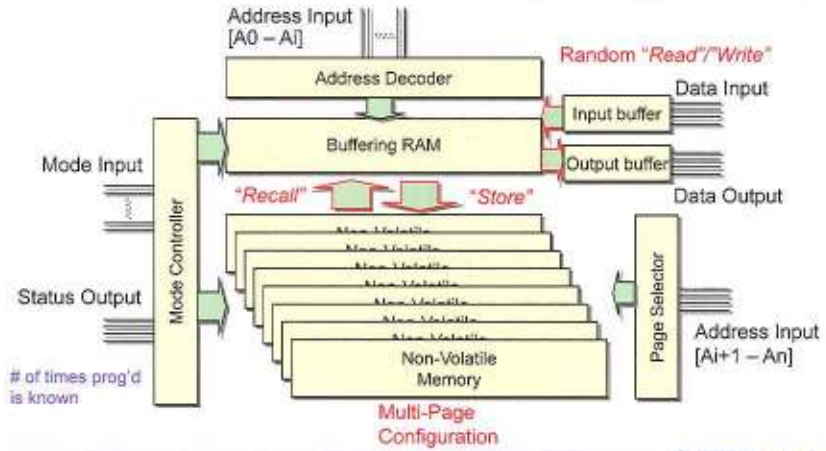
- *Process Generation: 0.13μm Process*
- *IO: 64b (configurable from 1b to 256b)*
- *Metal Usage: 3 Layers (no limitation on routing over the macro)*



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SRAM-Like Architecture for Large Memory Size

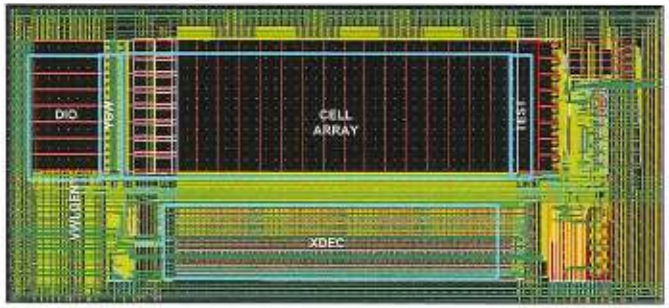


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16Kb OTP/4Kb 4-Time-Programmable

- *Process Generation: 65nm Process*
- *IO: 8b/16b/64b (pin option)*
- *Metal Usage: 3 Layers (no limitation on routing over the macro)*



(329um x 144um)

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OTP Memory Compiler

In 0.13 to 0.11μm generations, our OTP Compiler supports the following variations of memory size from 4Kb to 320Kb and IO pin count from 8 to 40.

		IO				
		8	16	24	32	40
		Column				
		64	128	192	256	320
Row	64	4,096	8,192	12,288	16,384	20,480
	128	8,192	16,384	24,576	32,768	40,960
	192	12,288	24,576	36,864	49,152	61,440
	256	16,384	32,768	49,152	65,536	81,920
	320	20,480	40,960	61,440	81,920	102,400
	384	24,576	49,152	73,728	98,304	122,880
	448	28,672	57,344	86,016	114,688	143,360
	512	32,768	65,536	98,304	131,072	163,840
	576	36,864	73,728	110,592	147,456	184,320
	640	40,960	81,920	122,880	163,840	204,800
	704	45,056	90,112	135,168	180,224	225,280
	768	49,152	98,304	147,456	196,608	245,760
	832	53,248	106,496	159,744	212,992	266,240
	896	57,344	114,688	172,032	229,376	286,720
	960	61,440	122,880	184,320	245,760	307,200
	1024	65,536	131,072	196,608	262,144	327,680



320Kb OTP Layout in 0.13μm Process

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MTP Technology

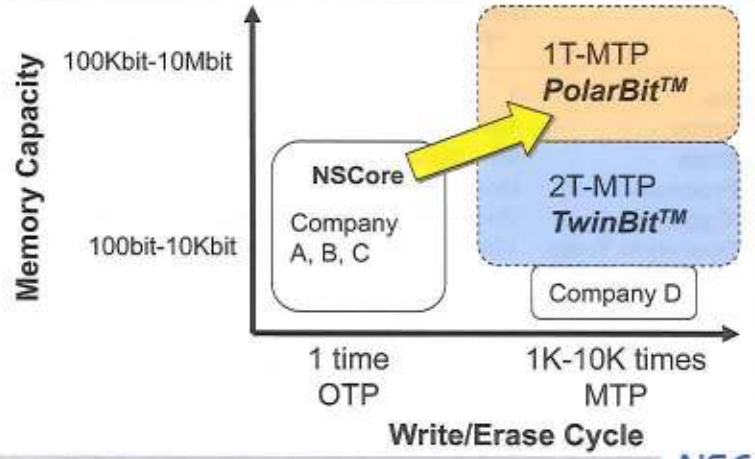
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Targeted Market Segment



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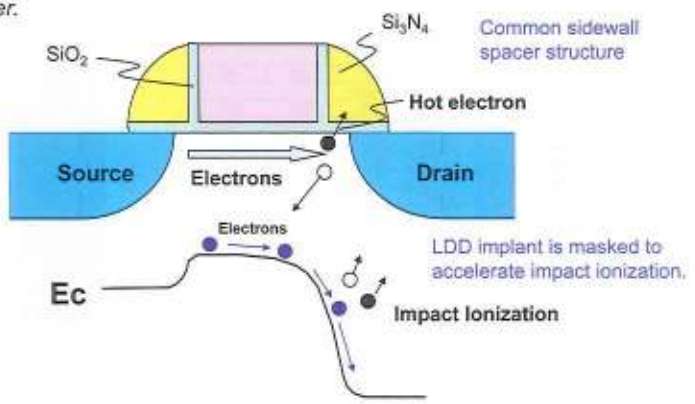
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In Program Operation

When nMOSFET turns ON, hot-electrons are generated and trapped in side-wall spacer.

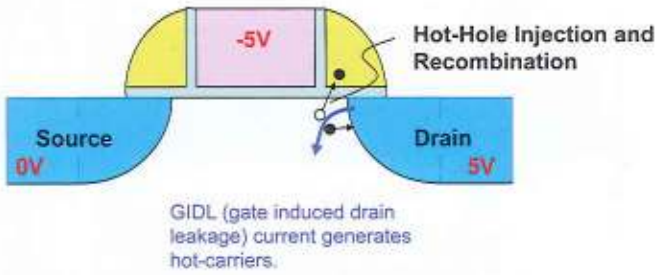


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In Erase Operation

When Gate is negatively biased, hot-holes are injected into the spacer and recombine with the trapped electrons.



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Technology Comparison

	NSCore's MTP "PolarBit"	e-Flash	Other CMOS MTP
Bit Area	1	2	20-100
Endurance	10-100K cycle	1K-10K cycle	100K cycle
Add. Mask	0/+1 Mask	+10 Mask	None
Add. Process	None	Stacked Poly	None
Read Cycle	30-50MHz	30-50MHz	30MHz
Max. Operation Temp.	125-150°C	125-150°C	125°C
Retention (10years@)	85-150°C	85-150°C	85-125°C
Program Voltage	5.5V	10V	20V
Read	Byte	Byte	Byte
Program	Block	Block	Byte
Erase	Block	Block	Byte

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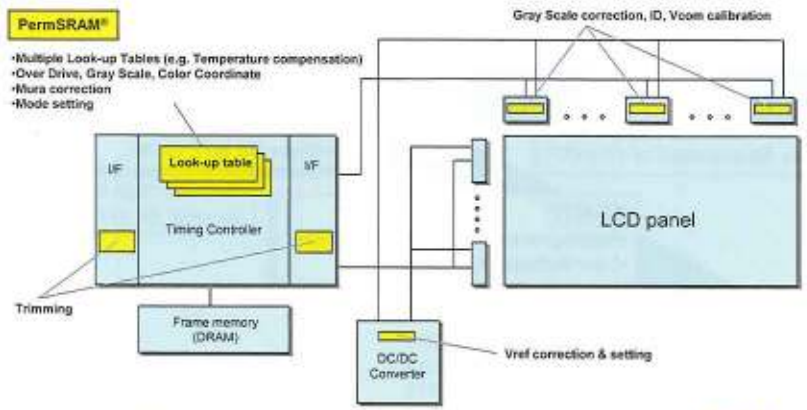
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Application Examples

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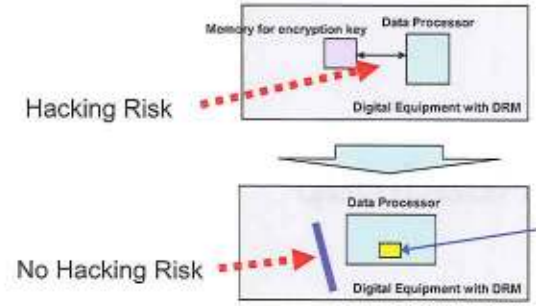
PermSRAM Applications (1)



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PermSRAM Applications (2)

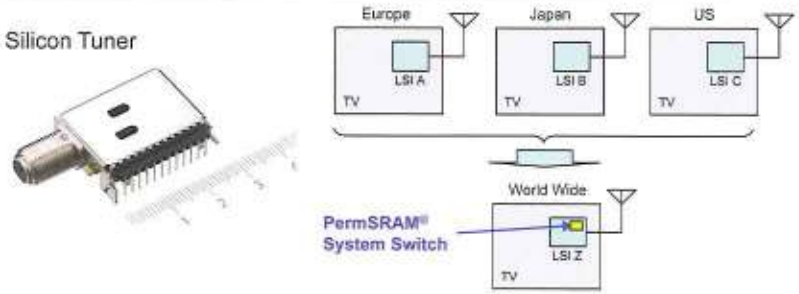


Benefit: Improved Data Sequrity
Low Cost
Small Volume

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PermSRAM Applications (3)

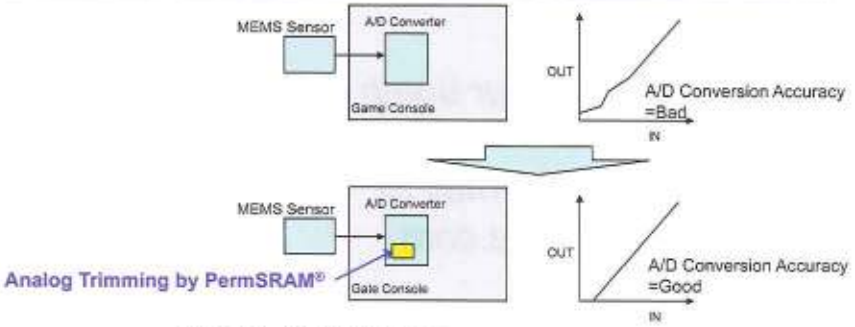


Benefit: Cost down for R&D
Cost down for Inventory Control
Cost down for Product Quality Control

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PermSRAM Applications (4)



Benefit: Small Volume
High Accuracy
Low Cost
Availability of Multiple Vendor Option for MEMS

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Roadmap

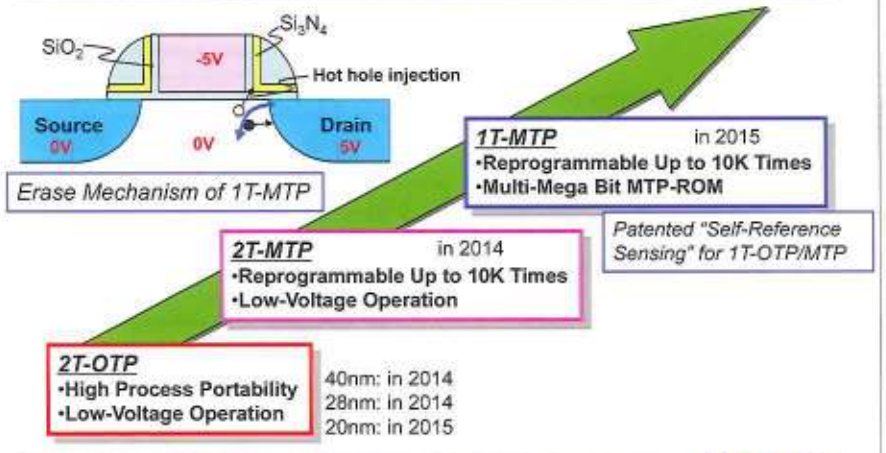
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NSCore's NVM Roadmap



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For more information

Please visit our booth #102.

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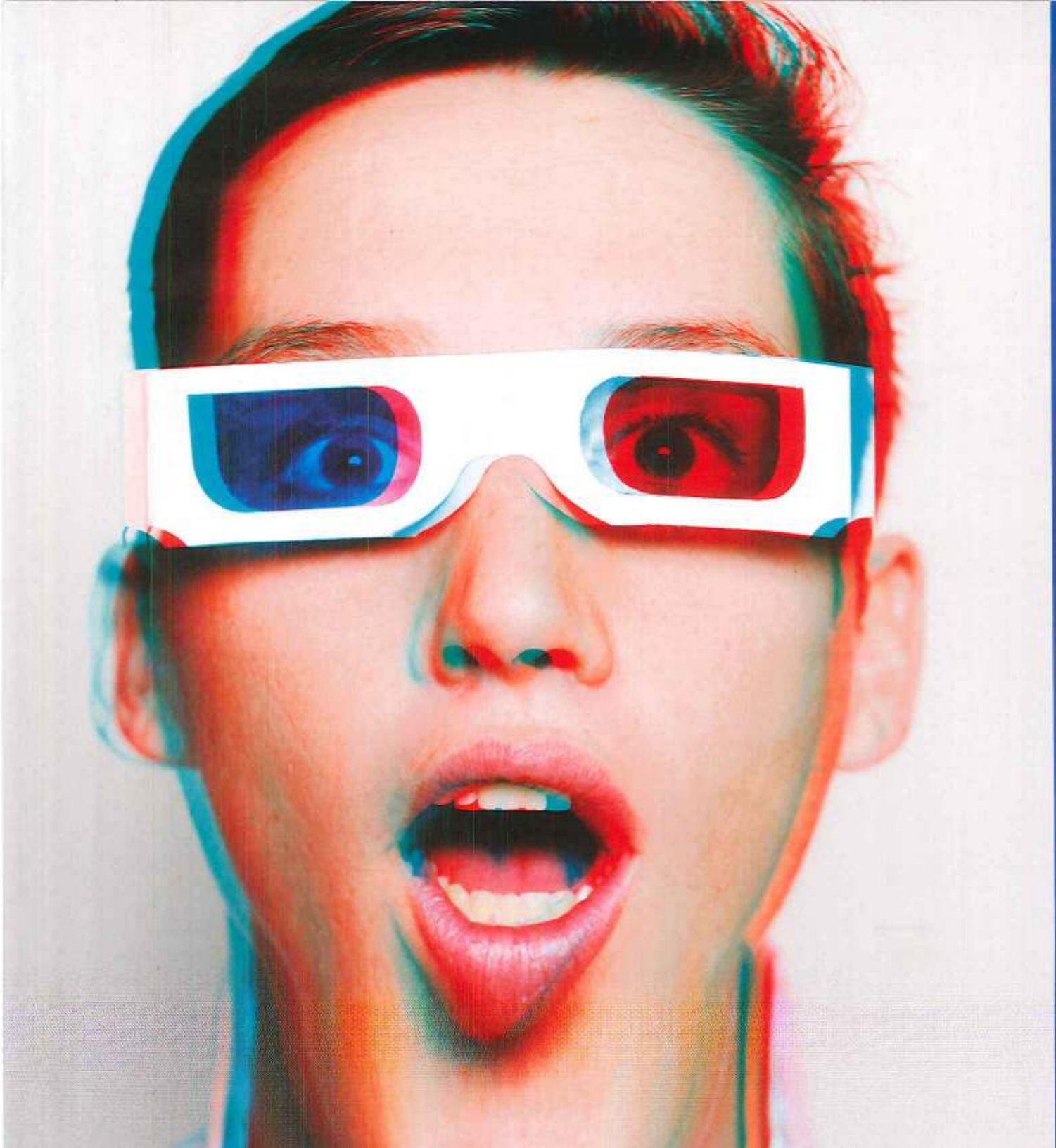
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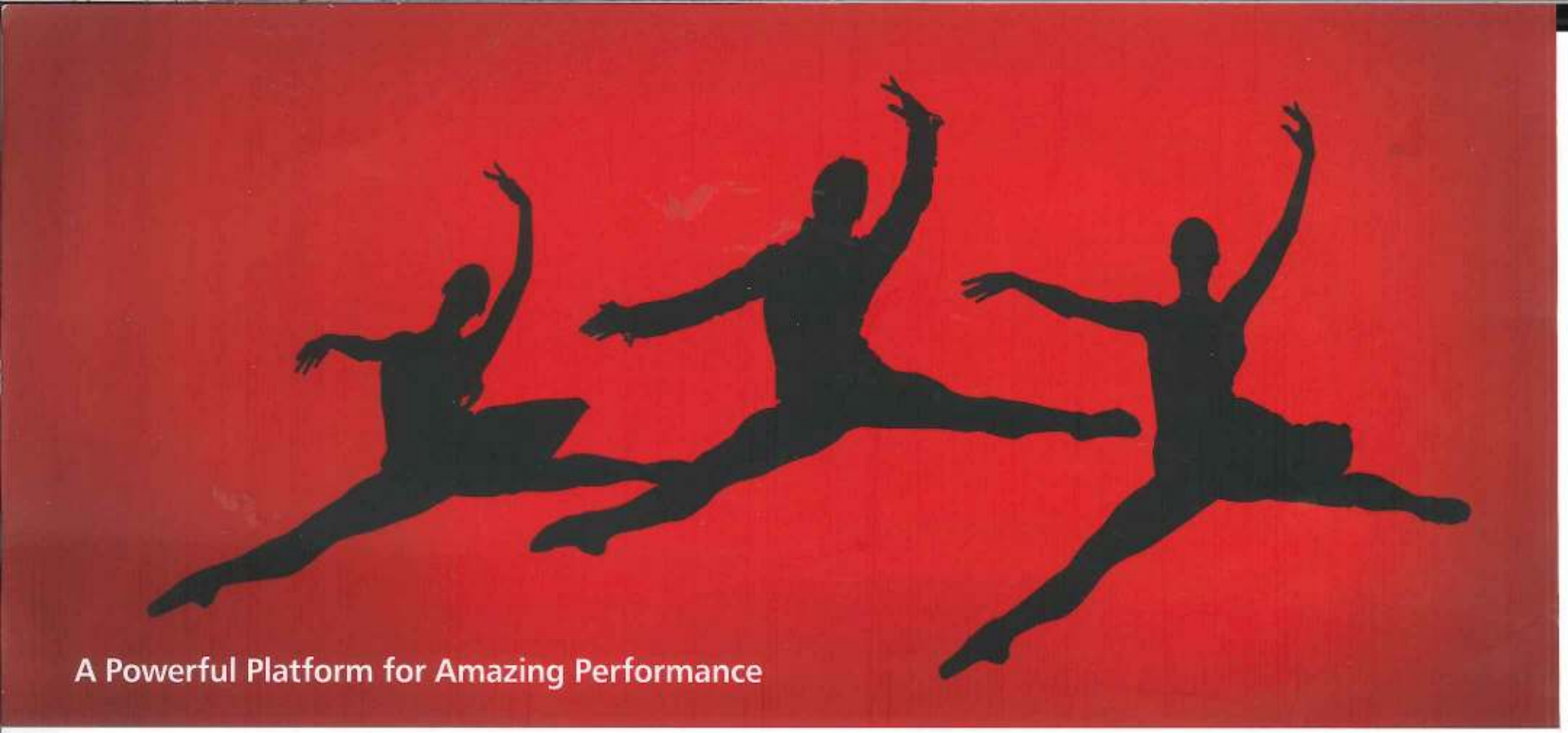
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